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Switched Zeta-Derived Topology Based On Modeling and Simulation for Lighting Load

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Abstract- High brightness white light emitting diodes (LEDs), has been attracted a lot of attention for general lighting applications conventional light bulbs in domestic, commercial, and industrial environments with high efficacy, longer lifespan, more compact size and environmental issues. The paper deals a quasi-active power factor corrector (PFC) and accurate current control for driving a string of HB LEDs. The proposed power supply for LED also is required for long lifespan, while maintaining high efficiency, high power factor, and low cost. However, a typical power supply design with an electrolytic capacitor as the storage operation, which is not only bulky, but also with a long lifetime, thus hampering performance correction of the entire LED lighting system. In this paper, a novel power factor correction (PFC) topology is employed by inserting the valley-fill circuit in the single-ended primary inductance converter (zeta)-derived DC-DC topology, which does not increase the voltage/current stress on the active switch used in the switching converter due to PFC. LED driver consist of diode bridge rectifier and resister to avoid the damage of LED by the higher current, because of this circuit is less efficient and approximately it is 20-30% efficient. This valley-fill zeta-derived topology operates in continuous conduction mode (CCM) in AC mains for universal input. Each LED has a 12V forward voltage and 0.25A forward current. There is some power quality indices such as total harmonic distortion of AC mains current (THD), distortion factor (DF), power factor (PF), crest factor (CF) and displacement power factor (DPF) are determine the characteristics of proposed LED lamp driver. The design, simulation and modelling of PFC zeta-derived DC-DC topology simulated in MATLAB/SIMULINK environment.

Keywords- Continuous Conduction Mode (CCM), Zeta-derived DC-DC Topology, Diode Bridge Rectifier (DBR), High Brightness White LED Driver.

I. INTRODUCTION

As Buck-Boost converter transfers almost all energy from input to output using the inductors and analyses is based on voltage balance across the inductor, hence Zeta-derived topology can be derived from the coupling of buck and boost topology and this topology utilizes energy of capacitance and on the current balance of the capacitor the simulation is based. Approximately 20-25% of total electrical energy is put into service employing artificial light sources by the entire world. Since past few years the advancement of technology in light looming around the more efficient light emitting diodes (LEDs) and used it as a source of artificial light because of its numerous advantages such as long life, high lighting efficiency, very economical and environment friendly due to less mercury contents, less cost of production, require low maintenance, easily dimmable, less affected by vibrations due to the robust structure. In the market power LEDs are available of disparate power ratings of 1W, 2W and 5W with various voltage and current ratings. Some New power LEDs are designed for nominal currents of 230mA forward voltage in the range of 5-15V. There are some LEDs recently available at very high cost, but it is economical due to long life tenure. LED is used to special types of diodes, the method for executing them is to subdue the forward DC current through the resistors, but this sort of approach is rendering less efficient because of tremendous amount of energy loss in the internal circuit of LED lamp

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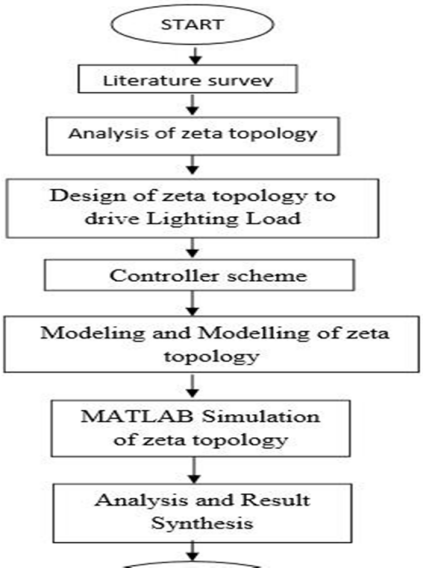


Figure: 1 Flow Chart of design for proposed topology

If primary source of energy is the AC then it will be mandatory to use some kind of AC-DC topology placed between the line and the high brightness (HB) LED. That is why, AC-AC converter is the relevant and suitable method to improve the power factor correction (PFC) or power factor re-regulators (PFP) of AC-DC converter. The commonly used power factor pre-regulators are boost, buck, buck-boost, SEPIC, CUK, and ZETA, also used for non-isolated and fly back is used for isolated mode. This can be operated in both continuous and discontinuous modes with better power quality at AC mains. In Figure 1 The systematic way of zeta-derived topology is illustrated.

II. LITERATURE SURVEY

Since LEDs are more reliable, have high brightness, less power consumption and long life, one decade ago Toshihiko and Nakagawa claimed that LEDs would work as lamp of next generation. They suggested an indoor communicating network which was acting as optical wireless communication system in laboratory associated with the white LED lights and was giving light in laboratory. Optical transmission and optical lighting both was taken care in the system. Receiver's FOV and data effect inter symbol interference for influence which degrades system performance. Potential of high speed transmission for data was proposed and FOV and data rate have been explained. In proposed system they distributed the light which irradiance is broad for function of equipment and claimed visible light system as LED lighting system for next generation. [1] A power factor corrected quasi active model was introduced to drive high brightness LEDs. It was able to work on power factor correction and two mode power balance. It was also claimed higher efficiency, reliability, low size, low cost and THD less than 10% without increasing stress on switch which was used for power factor correction. [2] A proposal came last year in which they claimed for better storage capacitance in power supplies for LED system. Since conventionally we were using electrolytic capacitor but in contrast Linlin Gu suggested use of film capacitor for getting better lifetime of power supplies. Power factor is sustained for whole input ranges that accepted internationally. They increased the ripple voltage of capacitor to get lesser capacitance which is stored already. They suggested different method of injection of third harmonic current for more change of storage capacitance. Eventually they claimed 65.6% reduction of storage capacitance with power factor of 0.9 and regulation standards of ENERGY STAR. To verify the suggested model they build a prototype for two-stage PFC converter wherein with help of storage capacitance the input output constant power and pulsating power is balanced. In experimental model voltage stress for switches was high. Ultimately they proved that the storage capacitance is affected by ripple voltage and suggested a other way to select an optimal value of capacitance. Also they suggested less pulsation for input voltage with help of third harmonic current injection method. [3-4] This model summate DC/DC stage and PFC front end circuit into single stage flyback for HB LED applications. 78W (24V-3.25A) prototype circuit showed efficiency of 87.5%, THD of 14% and power factor of 0.98 at input AC of 110Volt. [5]

A proposal came for LED ballast which consists of dual non cascading model of current-fed power factor correction pre-regulator. To get sustainable life time, they used low voltage capacitor in place of high voltage capacitor in the model. They

used programmed controller to improve power factor and they exploited the leakage inductance of transformer to reduce the stress on switch. Design proposed higher lifetime and efficiency due to its noncascading structure which is form by LED driver and secondary winding in transformer. [6]

Huang jen proposed dimmable LED driver where he used adaptive feedback system to control devices. To achieve higher efficiency and high power factor coupled inductor singled inductance PFC converter may be used with commercial transition controller [7].

The commercial ac voltage may be converted into pulsating current with double the line frequency to drive high bright LEDs using new idea of electrolytic capacitor less LED driver. By injecting fifth and third harmonics into input current they presented better lifetime of LEDs without electrolytic capacitor and reduced the peak to average output current ratio to 1.34 theoretically. They suggested power factor of more than 0.9 to meet worldwide standard using electrolytic capacitor less flyback topology with DCM mode in LED drive and derived duty cycle function in half line cycle. Finally they managed to construct prototype with output rating 25v, 0.35A and presented a better control method. Only 100Hz ripple in the LED current and AM dimming scheme was adoptable in their proposed model as limit. [8]

Taking the help of green SMPS controller TEA1750 IC from Philips for LED street lamp of 110Watt power a power LED driver circuit with capacity of 80volt/1.37A output was constructed. They affirmed benefit of quasi resonant, valley detection, low voltage protection, over voltage protection, over current protection, over temperature protection, 85% efficiency and PF of .94 within the standards of ENERGY STAR. [9]

After some years offline LED driver controlled by digital modular architecture was proposed. To get power factor of 0.9 they used low profile component with low voltage high frequency circuit and to achieve high efficiency and to reduce current ripples to 15% in the LED they employed bidirectional buck second stage. [10].

III. WORKING AND OPERATION OF ZETA-DERIVED TOPOLOGY

In the zeta-derived topology output voltage converted in to a DC voltage from the input with opposite polarity. Compared to the Boost, Buck and Buck-Boost converters the zeta-derived converter uses an additional capacitor and inductor to storage energy. There are following three modes of zeta-derived topology in sequence to the conduction state.

A. Switch-ON Mode: The current flowing through the inductor Lm increases linearly and the diode which are used in the circuit blocks in the on state.

B. Switch-OFF Mode: Since the current which are flowing through the inductor Lm cannot abruptly change and the diode must carry the current so it commutates and again starts to conduct. From the inductor Lm to the middle capacitor C0 energy is transferred and resulting in a decreasing inductor current.

C. Discontinuous conduction mode (DCM): In this state the current through the inductor Lm again starts to increases linearly and the diode again blocks. The middle capacitor discharges and supplies the RC load through the inductor L0. Across the resistor R the induced voltage has the opposite polarity of the input voltage. Waveform of zeta-derived topology is shown in Figure 2 [11].

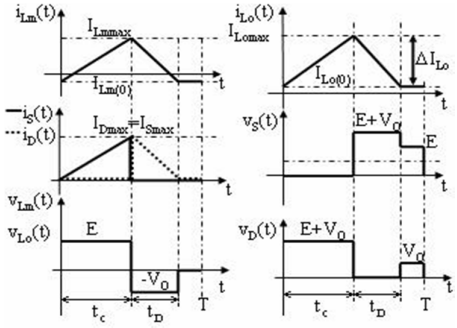


Figure: 2 Zeta-derived topology waveforms

The circuit which are used in the zeta-derived topology has two limits of operation. For a PWM duty cycle D → 0 the output voltage equals to zero, and in the other side for D → 1 the output voltage grows toward negative infinity. This equation (V_{out} = - D/ (1-D) • Vin.) is given for conduction mode of the output voltages that are the limits of the circuit. For the combination of inductors and capacitors acts as a second order low pass filter to just reducing the voltage ripple at the output. As compared to the previous dc to dc voltage topology (Buck, Boost and Buck-Boost) the zeta converter remains always allows continuous current flow through the inductors, and there are no any type of abducted discontinuous conduction mode is possible. The small

signal averaged state-space method is a either simple circuits or complex structures [12, 13]. By using mathematical analysis and effort, this method is helpful to achieve linear averaged time-invariant models and its derived final result. Procedure proposed by researchers [14, 15] is adapted here to obtain such models and to solve to our problem. The schematic diagram of Zeta-derived topology is shown in Figure 3

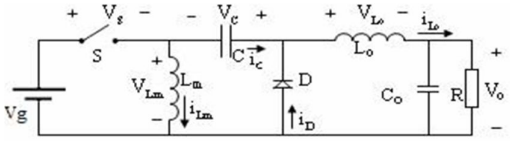
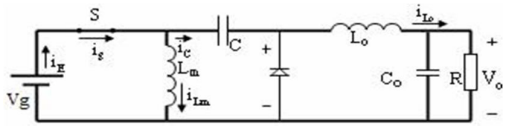


Figure: 3 Basic Circuit of ZETA Converter

The model has the mathematical description of the real system behaviour which is required to check the stability of that system. Here starting point is the extraction of state equation by using Kirchhoff's voltage and current laws for two operating modes of switch. First mode is when the switch is in on state and the diode is off, and the second mode is that the switch is off and the diode is on. All extracted state equation are obtained in first order and reduce the complexity of the equations and ease the analysis because these equations are calculated in nodes and loops in the presence of one passive element.



. Figure: 3 (a) ON State

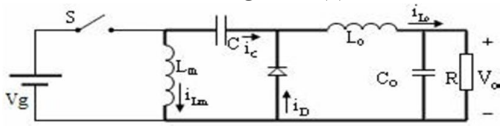


Figure: 3 (b) OFF State

IV. STATE SPACE EQUATIONS ANALYSIS OF PROPOSED TOPOLOGY

Provided that the natural frequencies of the converter, as well as the frequencies of variations of the converter inputs, are much slower than the switching frequency, then the state-space averaged model that describes the converter in equilibrium is

$$0 = AX + BU \quad Y = CX + EU$$

Where the averaged matrices are

$$A = DA_1 + D'A_2$$

$$B = DB_1 + D'B_2$$

$$C = DC_1 + D'C_2$$

$$E = DE_1 + D'E_2$$

And the equilibrium dc components are

X = equilibrium (dc) state vector

U = equilibrium (dc) input vector

Y = equilibrium (dc) output vector

D = equilibrium (dc) duty cycle

Equilibrium state-space averaged model

$$0 = AX + BU \quad Y = CX + EU$$

Solution for X and Y:

$$X = -A^{-1}BU$$
$$Y = (-CA^{-1}B + E)U$$

$$K\frac{dx(t)}{dt} = Ax(t) + Bu(t) + \{(A_1 - A_2)X + (B_1 - B_2)U\}d(t)$$

$$y(t) = Cx(t) + Eu(t) + \{(C_1 - C_2)X + (E_1 - E_2)U\}d(t)$$

$x(t)$ = small – signal (ac) perturbation in state vector $u(t)$ = small – signal (ac) perturbation in input vector $y(t)$ = small – signal (ac) perturbation in output vector

$d(t)$ = small – signal (ac) perturbation in duty cycle

To build a small signal ac model at an operating point, the duty ratio is considered as

Where D and are the constant and

The small signal ac model can be given by the following state equation

V. PROPOSED MODEL OF PFC ZETA-DERIVED TOPOLOGY BASED LED DRIVER

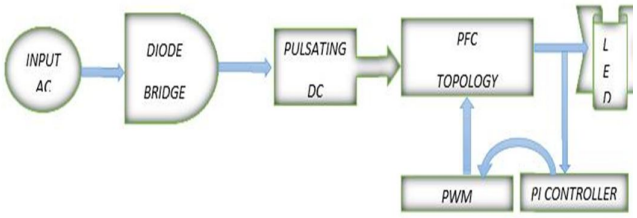
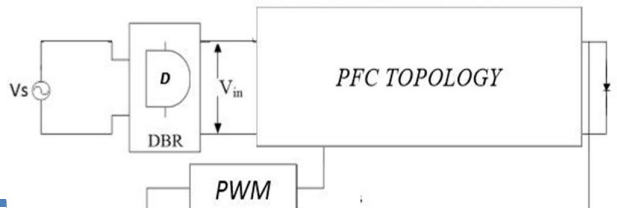


Figure: 4 Power Supply Flow

High brightness white light emitting diodes (LEDs) with universal input voltage needs the employment of Zeta-derived topology based power supply. In the suggested LED driver, power factor correction (PFC) AC-DC, AC mains helps to improve the input power factor to the required level as per the limits given by various international standards like IEC-61000-3-2 class D requirement. The zeta-derived maintains constant output lamp voltage to achieve stable operation of lighting driver to retrofit applications. The operation of PFC topology at high switching frequency reduces the weight and size of passive components like inductors and capacitors. PWM dimming technique is used to drive multiple LED lamps for universal voltage input**.** Below in Figure the block diagram of proposed LED driver is shown. An uncontrolled diode bridge rectifier (DBR) is arranged after input supply to generate pulsating DC signal that goes into PFC Zeta- derived topology as input signal. This zeta-derived is used to generate a DC output voltage which is compared with the reference voltage and obtained the error signal that works as input signal to PI controller again. The output of PI controller compares with saw tooth wave of suitable frequency at 50 kHz to generate the PWM pulses. The PWM pulse with repeating frequency f_s and conduction duty D drives to switch M which is a p-channel power MOSFET device. The switching period is $T=1/f_s$ so the switch-on period is DT and switch-off period is (1-D) T. when the switch M turned off, the current flows through the free-wheeling diode D and descends for whole switching –off period (1-D)T. In continuous mode, current I_o does not become zero before s witch M turned on but current becomes zero before switch M turned on again in discontinuous mode.



VI. DESIGN AND ANALYSIS OF PROPOSED PFC ZETA-DERIVED BASED LED DRIVER

Few considerations have to be taken to design and estimate the proposed topology of LED driver, those are mention;
All the components of proposed LED driver have considered as ideal components.
For maintaining the input voltage constant in one switching cycle, the switching frequency has selected much higher than AC mains frequency.
At the time of starting LED lamp has considered as an open circuit and a pure resistor during steady state operation.
DC link capacitor is considered as high enough so that In one switching cycle the DC link voltage can be maintained constant for a wide variation of input AC mains [16]
The analysis and design of PFC Zeta converter is presented in continuous conduction mode (CCM) of operation and calculation of components is mention below.
For a Zeta converter operating in CCM, the duty cycle is defined as below

(1)

The critical value of inductance Lm and L0 is determined by allowing the change in peak-to-peak ripple current to be 100% of the average output current. The critical value of inductances Lm and L0 are defined as,

(2)

The coupling capacitor (C) is designed on the basis of its ripple voltage contents. The voltage across coupling capacitor is equal to the peak value of the input voltage. It's important to design the capacitor C and its value can be expressed as below,

(3)

To maintain DC output constant voltage with less value of ripple contents, the output DC link capacitor C_0 must have enough high capacitance and must supply a continuous load current at high switching frequency. The value of capacitor C_0 is expressed as below

(4)

where, the maximum value of AC mains input voltage is V_{in}, duty cycle is D, DC link voltage is V_{dc}, average input current is I_0, switching frequency of the active switch is f_s, the ripple voltage of coupling capacitor (i.e. $270\sqrt{2}$V) is ΔVc, the ripple voltage of DC link capacitor isΔVc_0. The minimum and maximum duty cycle are 0.307 and 0.413 at Ac mains voltage of 170 V and 270 V respectively using equation (1). switching frequency of 50 kHz and DC link voltage of 120 V and average load current Io= 723 mA, the calculated critical values of inductors from equation (2) are $L_m(crit) = L_0(crit) = 1.14$ mH (to ensure CCM operation selected as 2 mH)., V_c = 13% of V_c = 35.1volt, V_{c2} = 11% of V_{dc} = 13.2volt, The calculated value of coupling capacitor using equation (3) is C = 126.67 nF (selected as 120 nF) and from equation (4) the calculated value of DC link capacitor is Co = 436 µF for a voltage ripple of 13% (selected as 450 µF).

VII. CONTROL SCHEME

PI controller and pulse width modulator is used to control zeta-derived topology and constant the output voltage. System uses voltage control scheme and sends pulse to power switch
(M).

A. PI Controller

It controls the voltage which senses the output voltage (V_{dc}) and compares with the reference voltage (V_r) to obtained error voltage signal (V_e).
The output of PI voltage regulator at n^{th} sampling instant can be given as,

$I_c(n) = I_c(n-1) + K_p\{V_e(n)- V_e(n-1)\} + K_iV_e(n)$ Where, K_p and K_i are the proportional and integral gains.

B. PWM Signal Generation[13, 14]

It reduces the current harmonics and to obtained unity power factor, the input supply current must follow the shape of input

voltage. PWM signal is generated by comparing output of PI controller and fixed frequency carrier wave and works as gate input signal for power MOSFET switch of the PFC Zeta-derived topology.
If $K_c*I_c(n)$> carrier signal, then M=1 else M = 0.

VIII. MATLAB MODEL OF PROPOSED ZETA-DERIVED TOPOLOGY BASED LED DRIVER

The model of the proposed PFC Zeta converter based LED driver is developed in MATLAB/Simulink and it is shown in Figure 6 under normal running condition in which the lamp is considered as a resistor at high frequency.

Figure: 6 Model of Proposed Zeta-derived Topology Based on LED Driver

technique is used to operate it in continuous condition mode (CCM). The switching frequency is 50 kHz to generate PWM pulses which works as gate input to on the solid state power switch. The designed- values of the Zeta converter components obtained from equations (1)-(4) are selected appropriately to obtain better power quality improvement at universal input AC mains [15].

VIII. RESULT AND DISCUSSION

The main motive of design, modelling and simulation is to validate the performance of proposed PFC based LED driver which has low THD of AC mains current for the wide input voltage applications. The DC link voltage is kept almost constant at 120 V using closed loop control, thus the output current is maintained constant throughout the universal input voltage range (170V-270V), which realizes the constant power. Figures 7 show waveforms, Output voltage (V) Power factor and Harmonic distortion at 170 V under normal running conditions.

Figures 8 Show waveforms, Output voltage (V), Power factor and Low Harmonic distortion at 220 V under normal running condition.

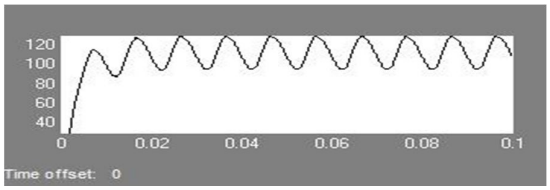


Fig: 7(a) Output voltage at 170 input voltage

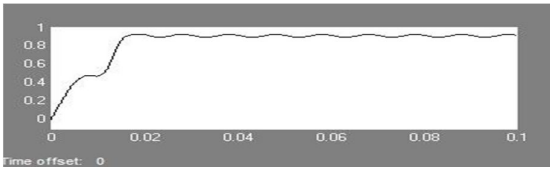


Fig: 7(b) Power factor at 170 input voltage

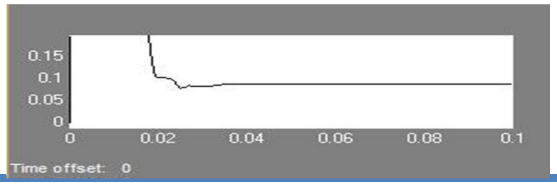


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Fig: 7(c) Harmonic distortion at 170 input voltage

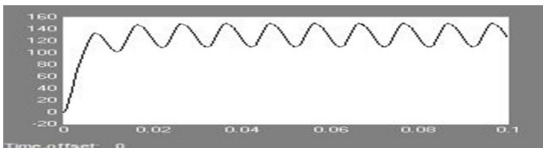

Fig: 8(a) Output voltage at 220 input voltage

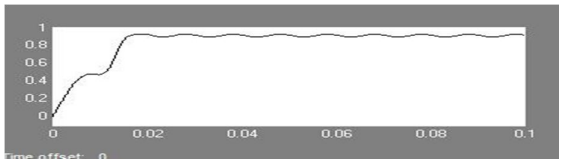

Fig: 8(b) Power factor at 220 input voltage

The topology based on PFC Zeta-derived topology is modelled in the MATLAB-Simulink toolbox where Proportional Integral (PI) controller where voltage follower

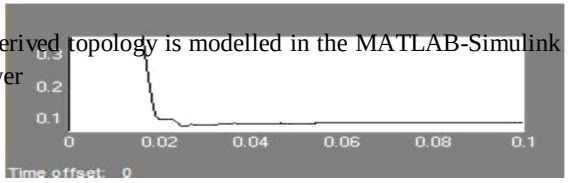

Fig: 8(c) Harmonic distortion at 220 input voltage Table-I Highlights power factor variations and % THD variations of AC mains of proposed model with the range of input voltage. The power quality indices of the proposed are found under the specified limits of strict international standard IEC61000-3-2 for class C equipment.

Table: I Simulation Performance Indices Result of Proposed Zeta-derived Topology Based LED Driver

V_{in}(v)	I_{in}(A)	P_s(w)	V_{out}(v)	I_{out}(A)	PF	THD
170	0.1035	17.56	120.73	0.2456	0.9985	2.45
180	0.0987	17.74	121.10	0.2469	0.9990	2.10
190	0.0942	17.87	121.38	0.2478	0.9987	2.95
200	0.0902	18.01	121.64	0.2488	0.9987	2.27
210	0.0863	18.09	121.81	0.2493	0.9985	2.34
220	0.0829	18.19	122.00	0.2500	0.9974	3.62
230	0.0797	18.25	122.12	0.2504	0.9959	3.82
240	0.0782	18.70	122.24	0.2508	0.9964	4.01
250	0.0737	18.35	122.32	0.2511	0.9961	4.49
260	0.0711	18.40	122.40	0.2514	0.9957	5.47
270	0.0686	18.42	122.48	0.2517	0.9948	5.91

IX. CONCLUSIONS

A CCM operated PFC Zeta-derived topology based LED driver has been designed, modelled and its performance has been simulated with improved power quality for universal AC mains. The proposed LED driver with PFC Zeta-derived topology has shown good performance such as nearly unity power factor and crest factor of 1.35 for the universal AC mains. The current harmonics and input power factor of the proposed LED driver are have been found as per norms of strict mandatory international regulation IEC 61000-3-2 for Class-C equipments and IEEE-519. The DC link voltage has been maintained constant, which realizes the constant lamp voltage and subsequently constant lamp current for retrofit applications irrespective of the change in AC mains voltage. The lamp power has also remained constant for the complete variations of the input voltage. The proposed driver has low THD of AC mains current for the voltage range of 170V-270V. For the complete input voltage range the LED lamp current has not crossed the rated lamp current value of 724mA, which ensures the safety of LED module.

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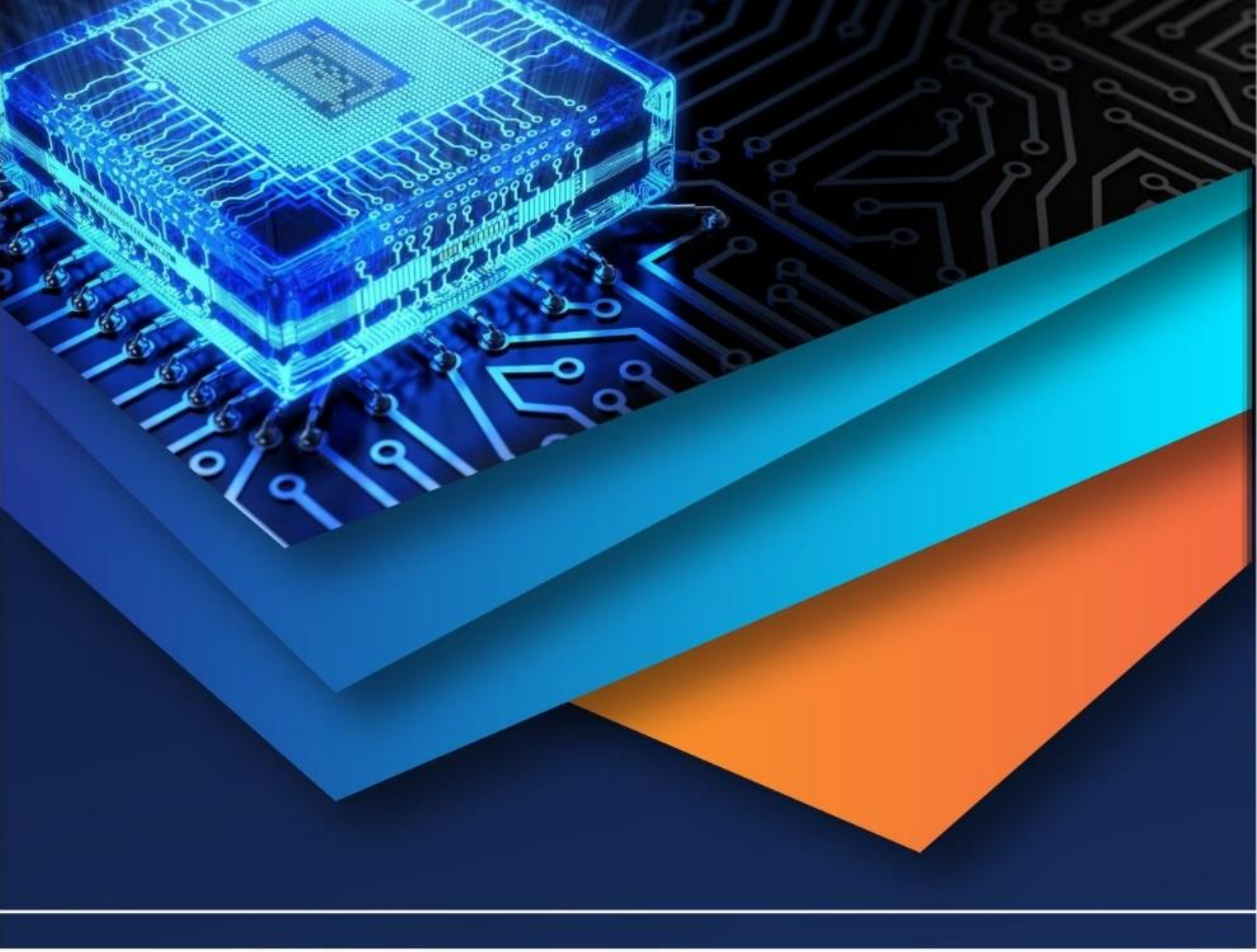

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