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Future MOSFET Devices using high-k (TiO_2) dielectric

Prerna

Guru Jambheshwar University, G.J.U.S. & T., Hisar,
Haryana, India, prernaa.29@gmail.com

Abstract: *In this paper, an 80nm NMOS with high-k (TiO_2) was designed and fabricated to study its electrical characteristics. ATHENA & ATLAS module of SILVACO software are used in simulating the electrical performance of the transistor. The parameters under simulation were the threshold voltage (V_t), I_d-V_g & I_d-V_d Characteristics. High-k gate technology is a strong alternative for replacing the conventional SiO_2 gates in MOSFETs for both high performance and low power applications. High-k oxides offer a solution to leakage problems that occurs as the gate oxide thickness is scaled down. Non-ideal effects such as short channel effects mainly channel modulation and drain induced barrier lowering (DIBL) are investigated in it. It is observed in the results that the threshold voltage could be varied by changing the above mentioned device parameters. The effectiveness is also observed on performance parameters of the MOSFET such as drain induced barrier lowering, sub-threshold slope and threshold voltage. Hence device engineering would play an important role in optimizing the device parameters.*

Keywords: *MOSFET, SCE-short channel effect, High-k, DIBL-drain induced barrier lowering.*

1. INTRODUCTION

Since the advent of MOS devices over 40 years ago, SiO_2 has been used as an efficient gate dielectric. The need for increased speed at constant power density has led to shrinking of MOSFET dimensions and as per scaling rules; the oxide thickness is also reduced in step. With scaling reaching sub nanometer technology nodes, the introduction of novel materials became inevitable as scaling of SiO_2 raises a serious concern in terms of tunneling current and oxide breakdown [7].

In order to prevent direct gate tunneling in very thin oxides, the SiO2 is replaced by alternative materials with higher permittivity and greater physical thickness. However, the introduction of these high-k dielectrics posses several problems, such as bi-dimensional electrostatic effects which may have a dramatic impact on the device performances when the gate dielectric thickness becomes comparable to the device gate length [7].

In this paper section 1.1 contains a description about High-k dielectric (TiO_2) while section 2 describes the design and simulation of N-channel MOSFET device with all the results and analysis discussed in section 3.

1.1 Titanium Dioxide (TiO_2) as gate dielectric.

TiO_2 has been used as an alternative gate dielectric material for deep submicron MOSFET's earlier in 1995 [2]. Advantages: The dielectric constant of TiO_2 is 80. The bandgap of the material is 3.5eV for amorphous films and 3.2eV for crystalline films. These band gaps are good for semiconductor but higher bandgap is required to act as an effective insulator [2].

The TiO_2 has low energy band offset with respect to Si. TiO_2 has EOT of less than 10Å. Transistors made with TiO_2 shows near ideal behavior but they have challenges with mobility. It has been shown that the low field effective mobility is approximately 160cm^2/V-s, which is about a three order lower than the mobility in SiO_2 based MOSFET's. This mobility reduction is due to interface trap state and surface roughness at TiO_2/Si interface. The electron traps in TiO_2 is due to oxygen vacancy. An empirical relationship between the effective mobility and the interface state density which is given by [2],

$$\frac{\mu}{\mu_0} = \frac{1}{1+\alpha D_{it}} \qquad (1)$$

where D_{it} is the concentration of charged states at the bias condition and α is a constant. So the effective mobility is inversely related with D_{it} [2].

In Si/SiO_2 interface bond strain causes fixed charge which is about 0.1% of the interface atoms (10^{10}-$10^{11}cm^2$). So for strained-Si/TiO_2 leakage occurs from these defects as well as from low conduction band discontinuity. Therefore, ultra-thin SiO_2 can be incorporated between TiO_2 and strained-Si layer to reduce the defect states at the interface. Therefore if TiO_2 is grown on (100) Si substrate D_{it} decreases and the mobility increases [2]. Mobility also can be increased by growing TiO_2 gate dielectric stack on Si substrate. The device speed can be improved by 20-80% at a constant gate length by using high mobility strained-Si at the channel region. TiO_2 reduces gate leakage and Si enhances the device speed [2]. Hence TiO_2 is our choice of high-k dielectric gate material. The other high-k materials are shown in table-1 [2] with their properties along with TiO_2.

Table 1: High-k dielectric materials and their properties.

Gate dielectric Material	Dielectric constant (k)	Energy bandgap Eg (eV)	Conduction band offset ΔEc (eV)	Valence band offset ΔEc(eV)
SiO_2	3.9	9	3.5	4.4
Al_2O_3	8	8.8	3	4.7
TiO_2	80	3.5	1.1	1.3

ZrO_2	25	5.8	1.4	3.3
HfO_2	25	5.8	1.4	3.3
Ta_2O_5	25	6	1.5	3.4
Y_2O_3	13	6	2.3	2.6
Ya_2O_3	27	4.3	2.3	0.9

2. DESIGN & SIMULATION

Simulations are performed with a two-dimensional (2-D) device simulator, SILVACO. The physical structure of the high-k NMOS used in our present study are designed using ATHENA considering the standard Silicon Integrated chip processing technology and the electrical characteristics are simulated using ATLAS device simulator.

The specifications of the Silicon substrate considered for the design are p-type Boron doped substrate with doping concentration of 1 x 10^{18} atoms cm^{-3} and <100> orientation. The design structure consists of TiO_2 dielectric with Polysilicon gate is considered to explore the advantages of TiO_2 over SiO_2 dielectric. The simulated structure, which are based on fully scaled 80 nm gate length MOSFET's proposed in the ITRS, have gate length of 80 nm, with effective oxide thicknesses (EOT) of 2nm [4]. The dielectric constant of TiO_2 gate dielectric was considered to be 80. Steep retrograde channel doping is used with surface doping concentration of 8 x 10^{13} cm^{-3}. The complete summary of NMOS process flow is given below in table 2.

Table 2: Summary of NMOS design features process flow.

PROCESS	NMOS Device
Initial substrate doping, N_a	Boron, B = 1 x 10^{18} cm^{-3}
Retrograde well	Boron, B = 8 x 10^{13} cm^{-2} E =200keV
Gate oxide thickness, t_{ox}	2.0nm
Source/drain extension	Boron, B = 9.5 x 10^{11} cm^{-2}
Halo Implantation	Boron, B = 3 x $10^{13}cm^{-2}$ E =20keV
Source/Drain implant	Arsenic, As = 5 x $10^{15}cm^{-2}$ E =60keV
Final Rapid Thermal (RTA)	1000^{o}C/1 sec

3. RESULTS & DISCUSSION.

The results of fabrication & simulation of 80nm NMOS can be viewed in the TONYPLOT is as shown below. Figure1 shows the electrodes are highlighted in this final structure of this NMOS device.

The complete structure now can be simulated in ATLAS to provide specific characteristics such as I_d-V_g & I_d-V_d curve.

The simulated device structure (figure 1) is a symmetric N-channel NMOS with following parameters mentioned in table 3.

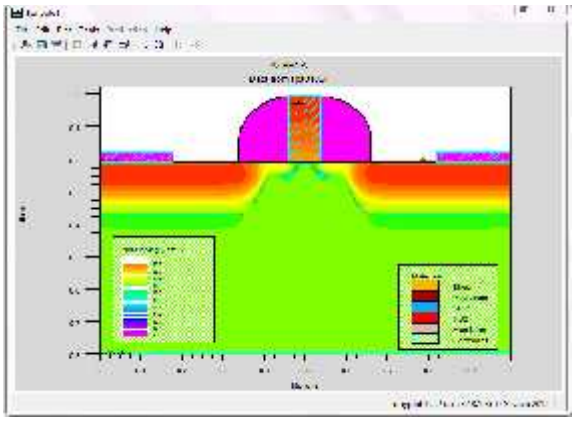

FIGURE 1 : COMPLETE STRUCTURE OF 80NM NMOS WITH TIO_2.

Table 3: Device parameters taken for process simulation of device design using ATHENA simulation tool.

PARAMETERS	NMOS
Sheet Resistance (Ω/square)	1624.31
Channel Surface Concentration (atoms/cm^3)	5.34893x 10^{17}
Gate oxide thickness, t_{ox}(nm)	2.0
Gate Length, L(µm)	.08
Gate Width, W(µm)	.2
Channel Length (µm)	.04
Channel Width (µm)	.3

The simulated NMOS structure with source/drain junction depth and net doping concentration is shown below in figure 2.

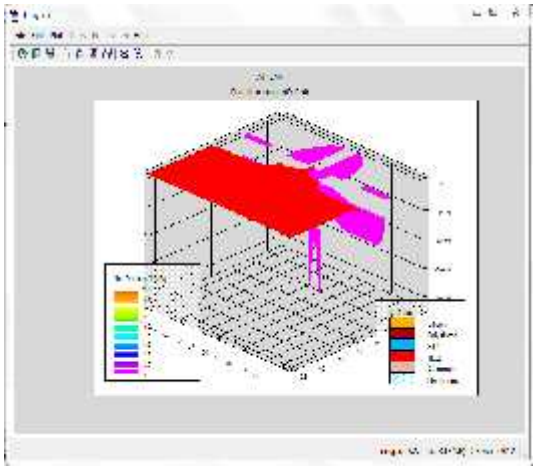

FIGURE 2 : NMOS STRUCTURE SHOWING THE JUNCTION DEPTH.

The complete structure can now be simulated using ATLAS to provide specific characteristics such as I_d-V_g, I_d-V_d, sub-threshold and DIBL curve.

Figure 3 shows that I_d vs. V_g curve, which gives the extraction of threshold voltage. The threshold voltage of this operation happens when the current reaches zero. V_d = -0.1V is applied for this graph. When $V_g<V_t$, the current is zero but the current start increasing when $V_g>V_t$. With a small value of V_d applied it is possible to examine the effect of an increase gate voltage. After reaching the threshold voltage the induced n-channel begins to increase in depth. The name enhancement type is tacked onto this type of MOSFET as a result of the gate voltage having to overcome the threshold voltage & enhance the channel [3].

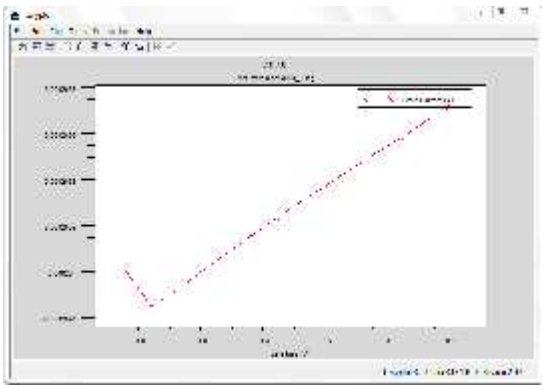

FIGURE 3 : THE I_D VS. V_G CURVE.

Figure 4 shows the families of I_d vs. V_d curves for NMOS. This curve is plotted using ATLAS simulator. The gate voltages that apply for 50.5V, 100.5V, & 150.5V denoted by red, green & blue lines [3]. The graph in figure 4 shows I_d -V_d not saturated due to the punch through effect only for Punch through causes a rapidly increasing current with increasing drain-source voltage. It is an extreme cause of channel length modulation where the depletion layers around the drain & source region merge into single depletion region. Suppose the red, green & blue line in graph start saturate at 0.2515V, 0.2517V & 0.2519V. But, this graph not saturate due to punch through effect [3].

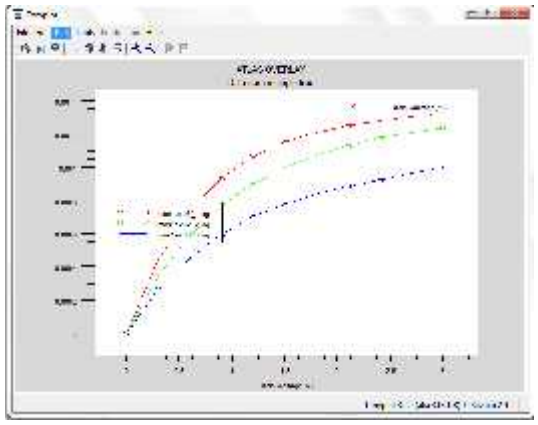

FIGURE 4 : THE I_D VS. V_D CURVE.

Figure 5 shows the sub-threshold characteristic curve for NMOS device with TiO_2 as gate dielectric. Sub-threshold characteristic of a MOSFET is an important parameter which determines the holding time in dynamic circuits as well as the static power dissipation in static CMOS circuits [5]. The sub-threshold current is due to weak inversion in the channel between flat-band and threshold voltage (for band-bending between zero and 2φF), which leads to a diffusion current from source to drain [6].

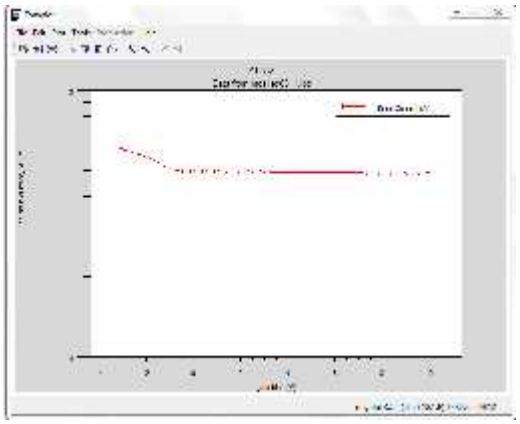

Figure 5 : Sub-threshold characteristic.

If small channel length MOSFETs are not scaled properly and the source/drain junctions are too deep or the channel doping is too low, there can be unintended electrostatic interactions between the source and the drain known as Drain Induced Barrier Lowering (DIBL). This leads to punch-through leakage or breakdown between the source and the drain, and loss of gate control [6]. A DIBL test is performed for the transistor, which results in a I_d-V_g plotted at different drain voltages (V_d). Figure 6 shows a decreasing DIBL curve for NMOS transistor with 0.025V and 0.05V drain voltage are shown by green & red curves respectively.

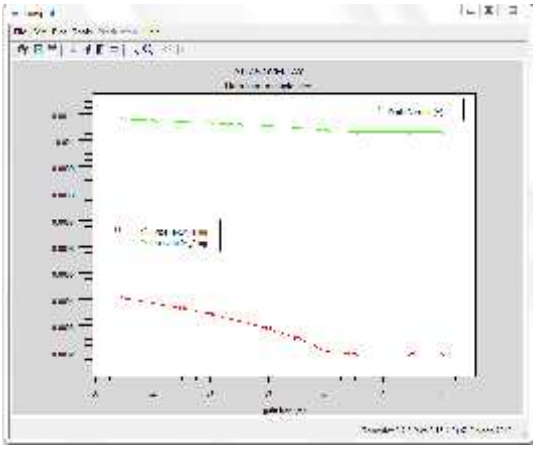

Figure 6 : DIBL curve.

3.1 Effect of drain voltage on threshold voltage

The value of gate to source voltage (V_{gs}) for which sufficient amount of mobile electrons accumulates in the channel region so that a conducting channel is formed is called the threshold voltage [7].

The Figure 7 describes the effect of drain voltage on threshold voltage for NMOS with TiO_2 gate dielectric. It is observed from the analysis that as the drain voltage increases, the threshold voltage decreases for NMOS. Thus, the threshold voltage of the device could be varied by applying different drain voltage to the transistor. However, a reduction in the threshold voltage gives rise to an increase in the sub-threshold leakage current, which is the current that is conducted through a transistor from its source to drain when the device is intended to be off. Due to this increase in sub-threshold current, static power consumption is increased and the overall device performance is degraded [1].

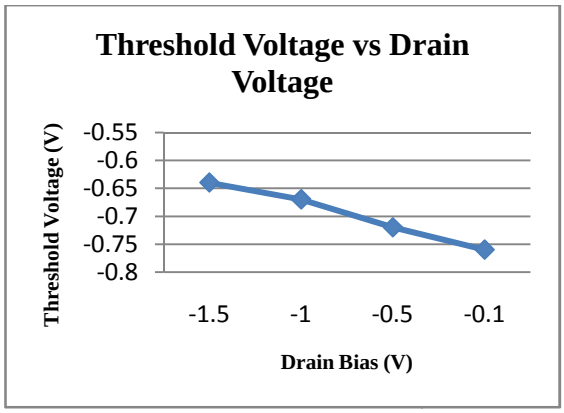

Figure 7 : Effect of drain voltage on threshold voltage.

An increase in threshold voltage is observed if the drain voltage applied to the transistor is quite low in magnitude, with an accompanying decrease in off state leakage current. Increasing the threshold voltage of the NMOS is an effective way to reduce sub-threshold leakage.

3.2 EFFECT OF GATE OXIDE THICKNESS ON THRESHOLD VOLTAGE

Figure 8 shows effect of gate oxide thickness on threshold voltage by varying the gate oxide thickness from 2.0nm to 3.5nm. The gate oxide thickness was the first parameter that was modified. The value of gate oxide thickness was modified to get the gate oxide thickness value in line with ITRS guideline for 80nm device [2].

With Increase in gate oxide thickness, V_t increases. The gate oxide thickness is a reverse proportion to the gate capacitance. When the gate oxide capacitance goes down, which means that the gate has less control over the channel in order to invert the channel, the V_t will increase.

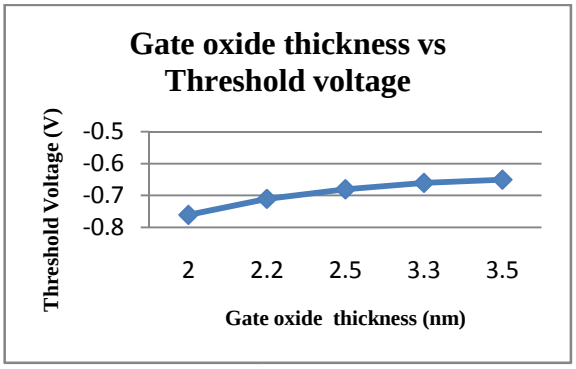

Figure 8 : Effect of gate oxide thickness on threshold voltage.

3.3 EFFECT OF GATE OXIDE THICKNESS ON SHEET RESISTANCE.

Sheet resistance is a measure of resistance of thin films that are nominally uniform in thickness. It is commonly used to characterize materials made by semiconductor doping, metal deposition etc. Examples of these processes are: doped semiconductor region (e.g., silicon or polysilicon).This parameter is applicable to two-dimensional systems in which thin films are considered as two-dimensional entities. This term implies that current flow is along the plane of the sheet, not perpendicular to it. Figure 9 shows effect of gate oxide thickness on Sheet resistance. With Increase in gate oxide thickness, sheet resistance decreases.

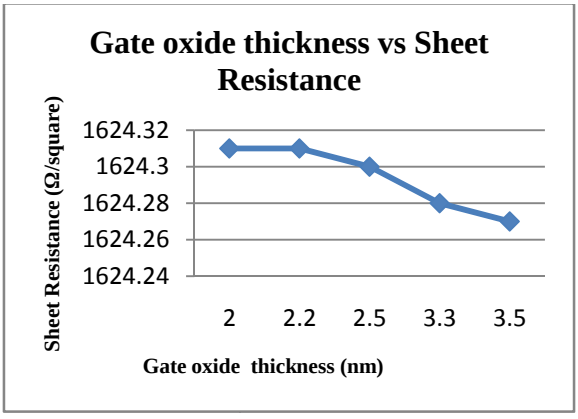

Figure 9 : Effect of gate oxide thickness on Sheet resistance.

3.4 Effect of gate oxide thickness on Channel Surface concentration.

Figure 10 shows effect of gate oxide thickness on threshold voltage. Here the gate oxide thickness is varied from 2.0nm to 3.5nm which proves that channel surface concentration increases with increase in gate oxide thickness.

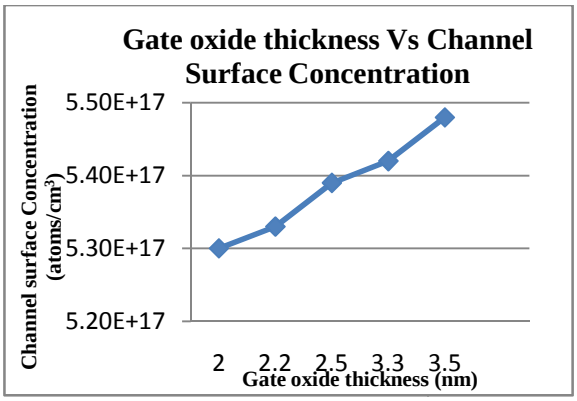

Figure 10 : Effect of gate oxide thickness on Channel Surface concentration.

The analysis of Threshold voltage, sheet resistance & channel surface concentration is studied for NMOS device. The summary of NMOS effect of gate oxide thickness on device parameters such as threshold voltage, sheet resistance, and channel surface concentration is shown in table 4 describing the above mentioned parameters are given below.

Table 4 : Summary of the effect of oxide thickness on device parameters for NMOS.

Gate Oxide Thickness (nm)	Threshold Voltage (V)	n++ Sheet Resistance (Ω/square)	Channel Surface Concentration (atoms/cm^3)
3.5	-0.65	1624.27	5.36551e+017
3.3	-0.66	1624.28	5.36324e+017
2.5	-0.68	1624.30	5.35432e+017
2.2	-0.71	1624.31	5.35108e+017
2.0	-0.76	1624.31	5.34893e+017

3.5 Effect of high-k (TiO_2) on threshold voltage

The high-k dielectric not only results in reducing the threshold voltage of the transistor but also reduces the major problem of short-channel affects i.e. Drain-Induced-Barrier-Lowering (DIBL). A comparison for both NMOS devices (SiO_2 & TiO_2 as gate dielectrics) with thickness of 80nm in respect with their threshold voltages (V_t) is shown in figure 11. Figure shows V_t for SiO_2 is 0.25V & for TiO_2 is -0.76V.

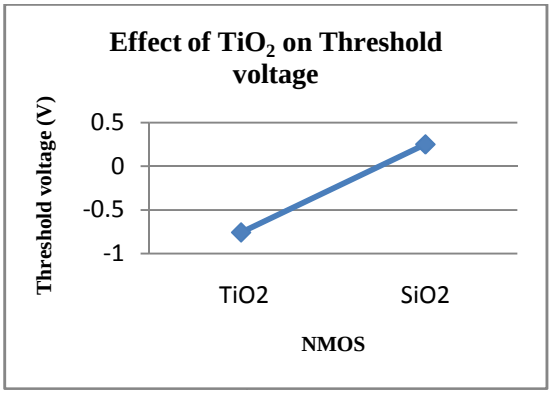

Figure 11 : Effect of TiO_2 on Threshold voltage.

It is of significant importance to reduce the sub-threshold swing, which is a measure of the rate of change in current (I_d) as a function of gate voltage (V_g) in a MOSFET, since a lower sub-threshold swing will lower the supply voltage and hence the dissipation [1]. From Figure 14 it can be observed that the sub-threshold swing (1/S) decreases when SiO_2 is replaced with TiO_2 dielectrics. This may be due to reduction in leakage current between drain and gate while using high-k dielectric material. The reduction in 1/S values with TiO_2 can also be attributed to heavy threshold adjust implants which blocks shallow paths for punch-through current thereby reducing 1/S in short channel devices [5]. The sub-threshold curve for TiO_2 is already shown in figure 5. I_d-V_g curve for NMOS with SiO_2 as gate oxide is also shown in figure 12 & DIBL curves for SiO_2 as gate dielectric is shown in figure 13. All these curves are plotted for 80nm SiO_2 gate dielectric N-channel MOSFET.

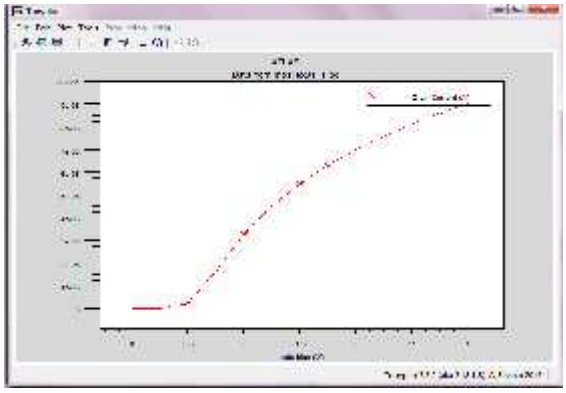

Figure 12 : I_d-V_g relation for 80nm NMOS with SiO_2 as gate oxide.

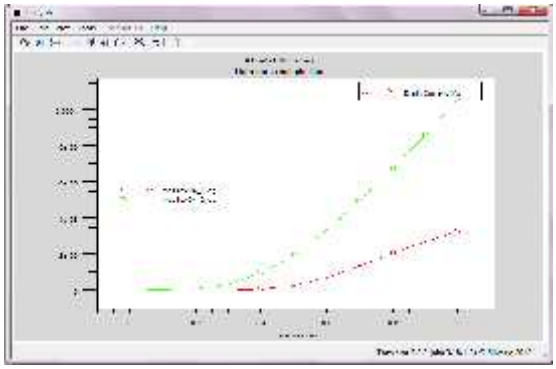

FIGURE 13 : DIBL CURVE FOR 80NM NMOS WITH SIO_2 AS GATE OXIDE.

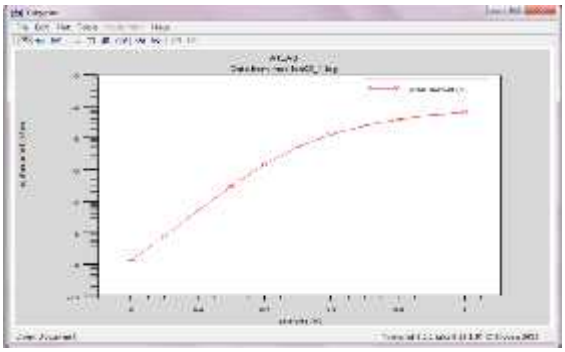

Figure 14 : Sub-threshold curve for 80nm NMOS with SiO_2 as gate oxide.

4. CONCLUSION

N-channel MOSFET structure with 80 nm gate length was designed and simulated to study the effect of high-k dielectric (TiO_2), drain voltage and oxide thickness on the device performance. Performance of the two structures- NMOS using TiO_2 with Polysilicon gate & NMOS using SiO_2 with Polysilicon gate were compared. It was found that some of the parameters like threshold voltage, sub-threshold swing and DIBL were reduced while drain current was increased upon applying high-k dielectric on planar MOSFET device structure. The sub-threshold leakage current was found to be decreased with increasing threshold voltage; this reduces the power consumption and thus improves the device performance. The reduction in gate leakage and sub-threshold swing projects the high-k MOSFET structure to be a strong alternative for future Nanoscale MOS devices. It can also be concluded from the analysis that as device was scaled down, the threshold voltage of the device decreases. Hence, to adjust the threshold voltage and other short channel effects within the permissible limits device engineering can be employed.

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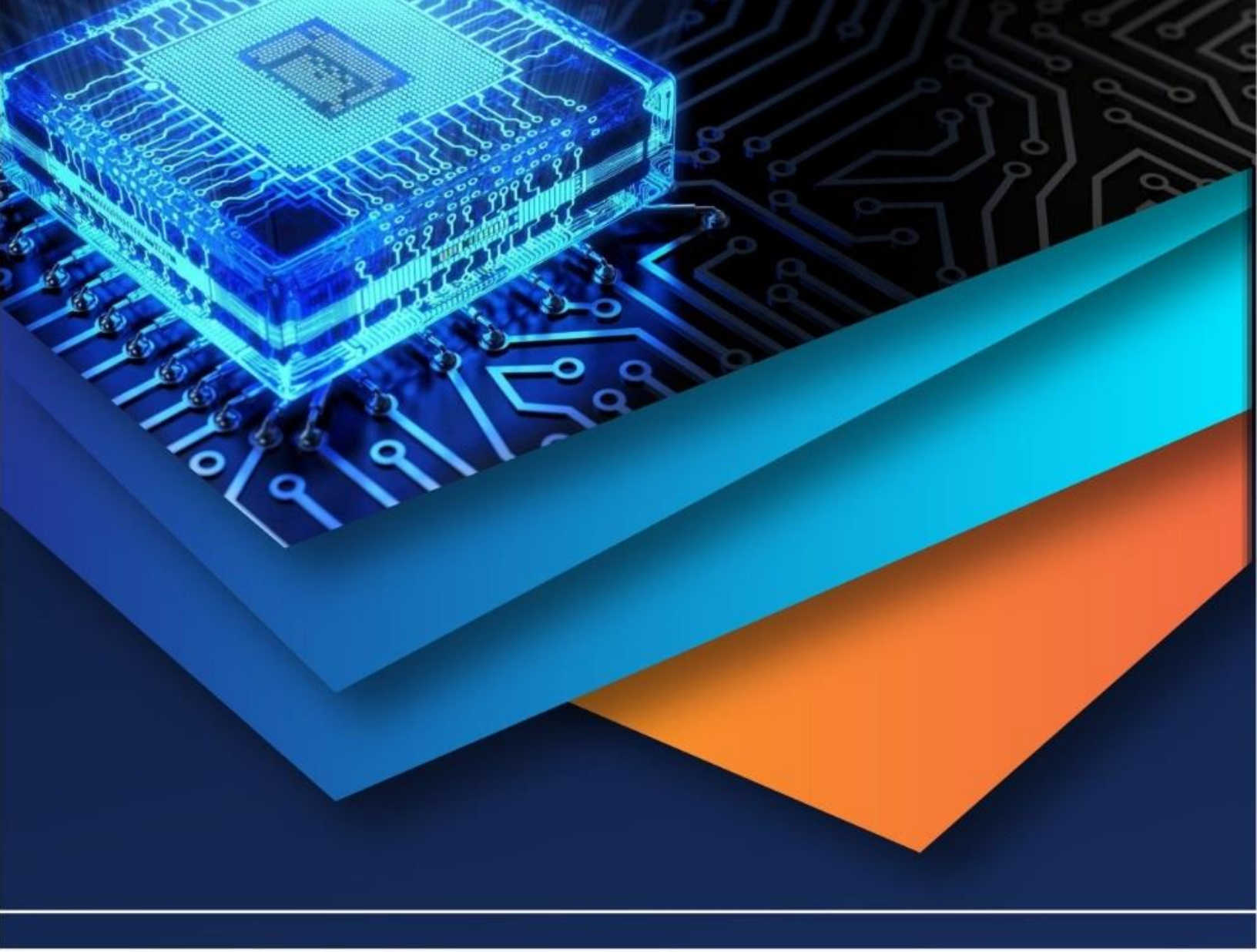

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