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# Design and Verification of Adaptive Router for NOC Using Buffer Resizing Technique

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***Abstract— This paper focuses on design of adaptive router with buffer resizing technique for network on chip(NOC) by run time reconfiguration of resources and verification of design using system verilog. Complex system on chip(SOC) designs requires high bandwidth interconnects, NOC provides solution with a relative area and delay overhead. Run time usage of resources improves performance and reduces area of NOC. Functional verification ensures the quality of silicon, 60% of design time is spent on verification. To overcome this verification delay the proposed design adopts latest verification methodologies. The design is verified using a reusable test bench written in system verilog. The design of adaptive router is developed in Verilog, synthesized and simulated in Xilinx ISE Design Suite 12.4 tool. The design is verified using system verilog using Questa SIM tool.***

***Keywords— NOC, SOC, FIFO, FSM, Verification.***

## I. INTRODUCTION

Network on chip is a on chip interconnection and communication concept that provides higher bandwidth, which is the basic requirement in complex designs. NOC provides a high level of parallelism by allowing simultaneous data transmission over all the links of NOC. This increases performance and reduces the latency. NOC is an attractive replacement for traditional bus based communication architecture or point to point dedicated links. NOC provides higher bandwidth and improved performance compared to traditional approaches but results in higher area and delay overhead.

NOC structure consists of processing elements, network interface cards and routers. Router includes switch, control logic and buffers. Buffers in routers consume most of the router area. NOC Router architecture optimization shows improvement in the overall performance of system. Buffers in the router influence the overall power consumption, area and performance of the NOC.

Resources such as buffers are used in different manner for different applications on the NOC. Some resources are necessary and sufficient for one application and they may be idle for other applications. In this way resources are under or over utilized depending on the application being executed on NOC. Proper utilization of these resources cannot be ensured at design time, hence runtime changes are needed. Considering the run time changes is the best way for efficient utilization of resources and improvement in overall efficiency of the interconnection network. Run time reconfiguration of network topology and routers leads to improvement in performance and overcomes the area and delay overhead. Dynamically changing the buffer size according to data traffic, routing algorithm and changes in switching technique are the possible runtime changes which can be implemented in adaptive NOC architectures.

As the system complexity increases, verification of these complex designs becomes a challenging task. Functional verification gives the quality of silicon hence 60% of the total design time is being spent on verification of designs which requires two times more verification engineers than design engineers. Direct test bench based verification is inefficient in complex designs and is time consuming. Most of ASIC re-spins are due to bugs in RTL design. There is a need for reusable, efficient methodologies which makes the functional verification easy and speedy, which can be achieved by adopting latest verification methodologies so that the verification phase can be accelerated.

In this paper, we introduce the router design for NOC and SOC applications, analyze the buffer resizing technique and importance of verification methodologies in section I. Section II, analyze the previous buffer resize techniques. Section III, the proposed adaptive router design, specification of the router and buffer resizing technique. Section IV, working of router with respect to input and output protocols. Section V, discussion on verification methodology and components developed for verification. Section VI, simulation results are discussed. Section VII, concludes the paper.

## II. RELATED WORK

Lan et.al proposes a buffer utilization technique by making the router channels bidirectional. This technique adds two extra tasks for the channel allocator: channel direction is dynamically configured depending on the request and allocating the channel to one of the

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channel sharing routers. This shows good improvement in the system performance but area overhead is increased up to 40% due to double crossbar and control logic design for bidirectional channels. We overcome the problem by using only one routing switch and simple arbiter logic to assign the buffers for ports. M. A. Al Faruque has proposed dynamic allocation of buffer blocks on traffic demand. This technique improves the latency and performance but area overhead reduces the overall efficiency of the system[1].
Concatto C proposed two techniques. First includes resource utilization at run time. In this approach a channel may borrow buffer units from its neighbour channels. This requires extra multiplexer logic for assigning buffers to one of the neighbouring channels. 6% area improvement can be observed with buffer size 4. Second technique, in which router adapts itself by providing proper size of buffer in terms of depth depending on the traffic requirement to maintain the performance with reduced power dissipation. This router consumes 30% less power but the extra resources needed increases up to 55%. But extra logic increases more than linearly with increase in size and hence solution is not scalable [2].

## III. THE PROPOSED ADAPTIVE ROUTER

Router is a basic building block of NOC which routes the incoming data from input port to the destination port depending on the address. In this design router operates on packet based protocol in which data is transmitted in the form of packets. Packet contains 3 fields: Header part, which contains 8 bit wide destination address, source address and length of data being transmitted. Length of data can be from 1 to 63 bytes. Data payload part contains the actual data that needs to be transmitted. Tail part contains the parity byte of 8bits calculated over header and data payload to ensure correct transmission and reception of data. The router has 5 ports out of which one is input port from where data enters the router and other 4 output ports, with unique port address to, which data is driven to and from where the data is received by actual device.

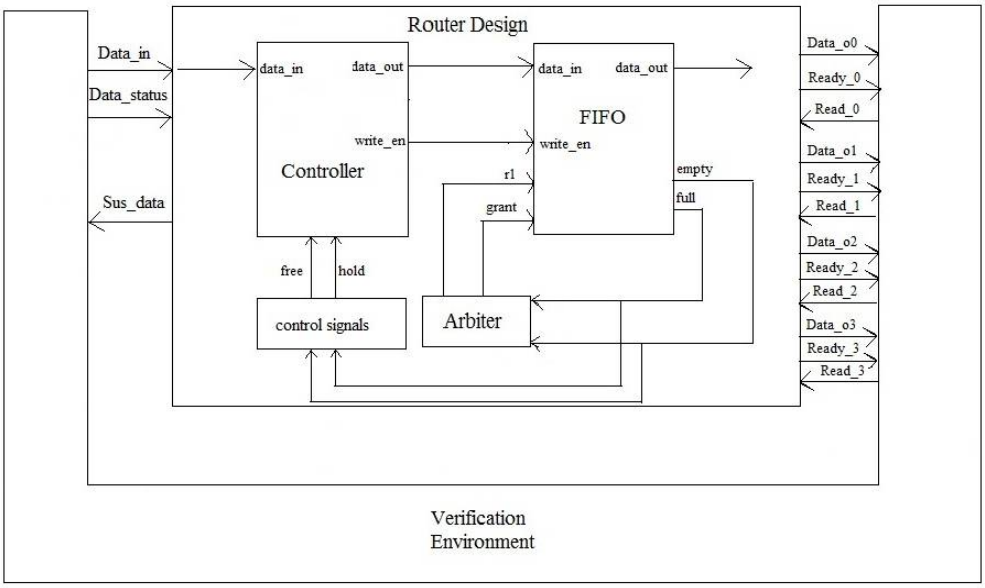


Fig. 1 Adaptive router

### A. *Buffer Resizing Technique*

When traffic congestion increases there exists blocking of data at destination ports due to lack of storage space. If two packets with same destination address enter the router and first packet is blocked due to lack of space then the second packet will also be blocked and it cannot be processed. This increases the latency of system and reduces the performance. Increasing the size of buffers can overcome the problem of packets being blocked. This change in size of buffer according to traffic demand is called buffer resizing technique. Resizing the buffer at run time that is, dynamically changing the size of buffer is called adaptive buffer resizing technique. In this approach we are using 4 static buffers and one floating buffer of same structure as static buffers. A buffer assigned to a particular port becomes full, then floating buffer is assigned to that port to store the further incoming data. This task of assigning floating buffers to ports is performed by arbiter as shown in the Fig. 1.

## IV. INPUT AND OUTPUT PROTOCOLS OF THE ROUTER

The router design is as shown in the above Fig. 1. It has one input port. Data_in and Data_status are input signals to router, if Data_status is high, inputs are driven into router through Data_in signal as shown in the Fig. 2. Router has 4 output ports each with

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three signals Data_out, Ready and Read. When valid data is available on the router then Ready signal is asserted, which is input to receiver. Read signal is asserted by receiver to receive the data from router this action performs read operation on FIFO. The read data is sent out to receiver through Data_out signal as shown in the figure3. When static FIFO becomes full, floating FIFO is assigned to port depending on FIFO full condition and address of the port. FIFO full and empty conditions are requests to arbiter it grants the write or read signals depending on the input or output operation respectively. When static FIFO and floating FIFO both are full and still there is data coming into router then it asserts Sus_data signal to suspend incoming packets.

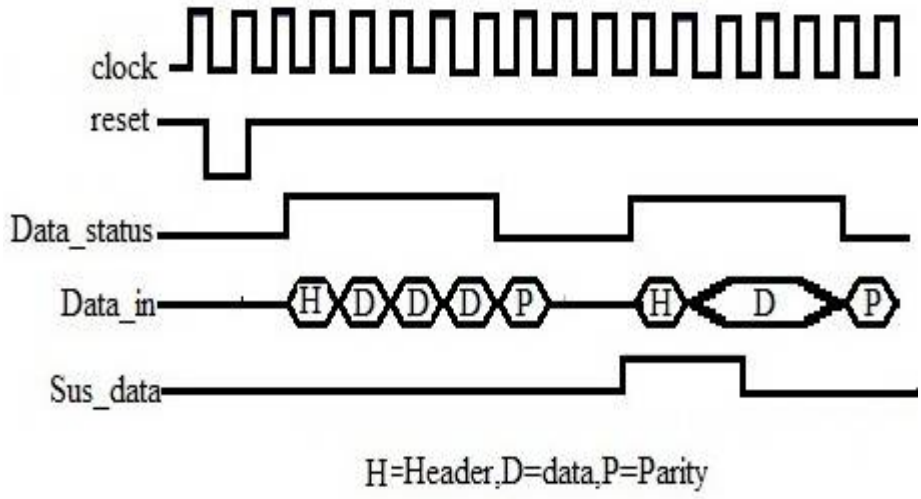


Fig. 2 Timing diagram of input protocol

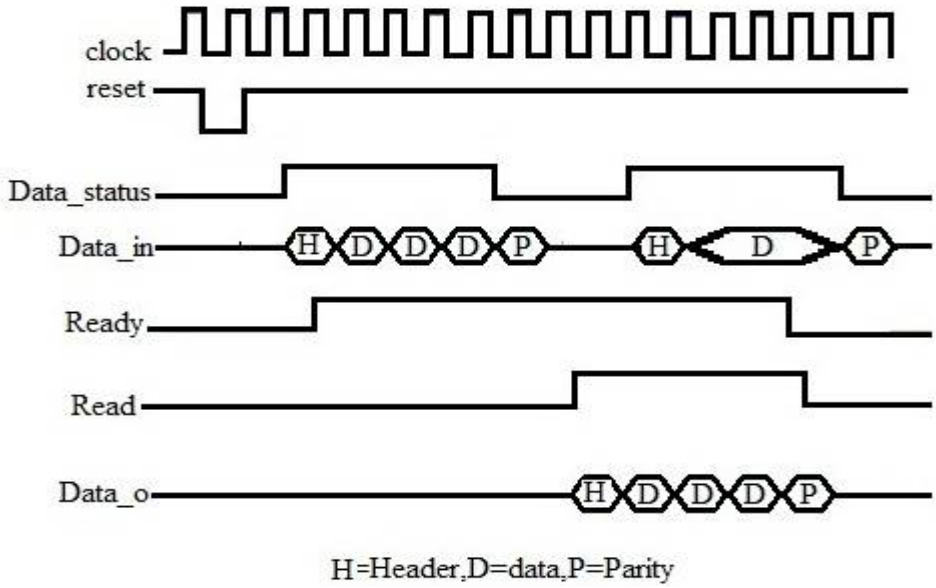


Fig. 3 Timing diagram of output protocol

## V. VERIFICATION

Verification is a process which is used to ensure that implementation of design reflects the intention of the design. As technology is improving there is a demand for small size , performance intensive and low cost devices. These requirements demands for the integration of multimillion gates and reusable IP cores on a single chip. Once the design is developed, verification of such complex designs becomes a tedious job, which consume 60% of design cycle time, and hence double the requirement of verification engineers than that of RTL design engineers. To overcome these challenges we need a verification methodology that can be reused which reduces the time of verification and in turn leads to shorter time to market.

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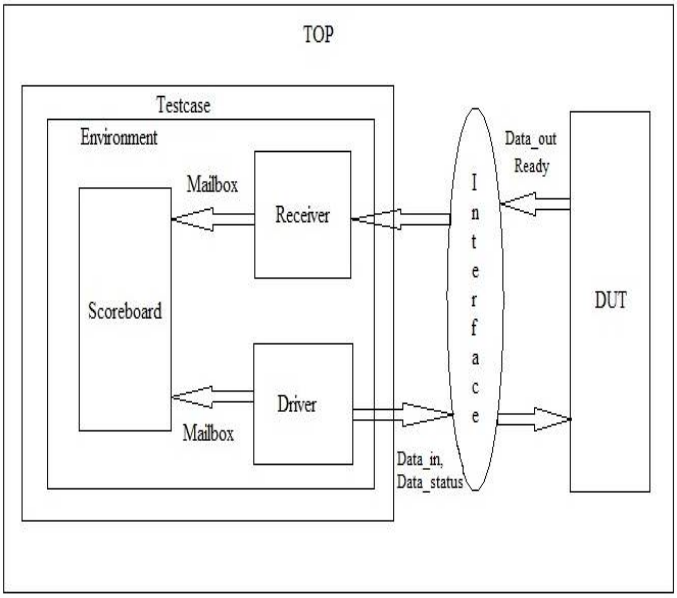


Fig. 4 Verification environment

For this router design we have developed the verification environment as shown in the above block diagram. Verification components used are: Driver to generate and drive input sequences to input the router that is Design Under Test (DUT) and the same sequences are sent to scoreboard through mailbox. Receiver collects the data on output ports and this data sent to scoreboard through mailbox. Scoreboard compares the incoming data from driver and receiver and displays the result in the form of packets matching. This ensures proper receiving of data at the receiver. Testcase is start point of testbench to verify the design and simulation is initiated at this point. Verification block and DUT communicate through the interface.

## VI. RESULTS

We have developed the design in verilog HDL using Xilinx ISE design tool. The same design is verified using the Questa SIM simulator using system verilog.

*A. RTL Schematic*

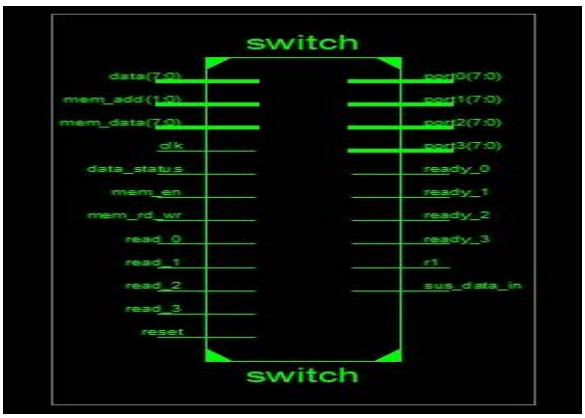


Fig. 5 RTL schematic of design

*B. Simulation Result*

From the below simulation result it is observed that when valid data appears on the router, Ready signal is asserted. The Read signal is asserted by the receiver to read the data on the output port. For better discussion and readability a FIFO with depth 6 is considered instead of 16. Two input packets of the size 11 and 6 bytes are considered here, in the first case a packet with total 11 bytes requires both static FIFO to store intial 6 data inputs and floating FIFO to store the remaining 5 inputs. In the second case a packet with total 6 bytes is considered, which requires only the static FIFO. If a static FIFO with depth 11 is used as in the regular

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router, this leads to under utilization of resource in the case of second packet. Hence by employing buffer resizing technique under utilization of resource is over come.

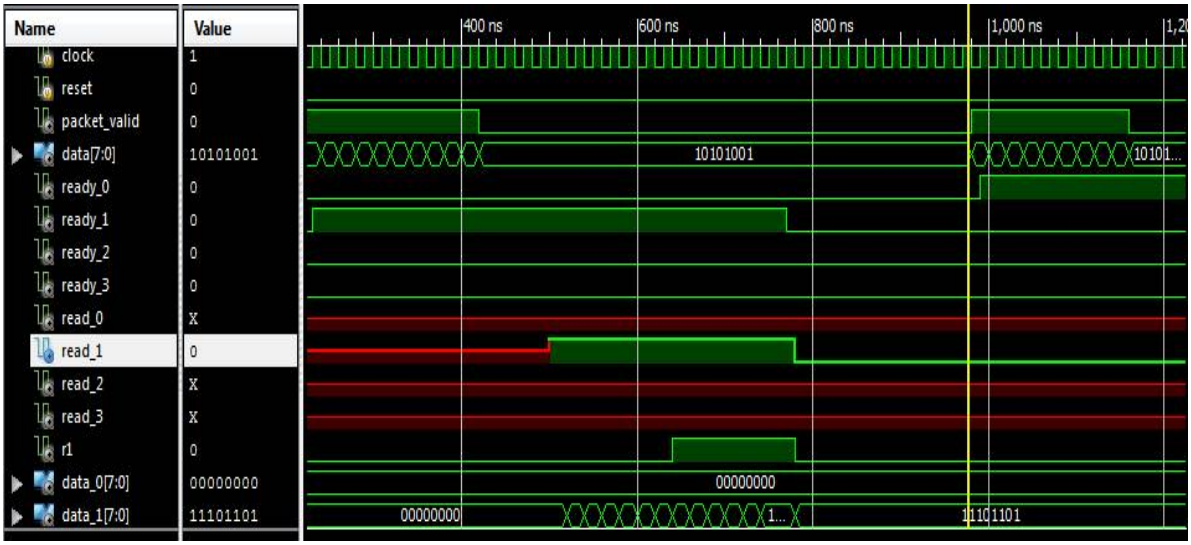


Fig 6: Simulation waveform

*C. Checker Output*

The router is verified by developing a verification environment. The input packets generated by driver are sent to DUT and checker. The output packets received from the DUT are sent to checker. Checker compares the individual bytes of the packets as shown in the below figure 5 and outputs the packets matched or not. If all the packets are matched then the test is passed. From the below figure 5 it is observed that driver is driving packet consisting of bytes 81,01,07,76,3d,ed,8c,f9,c6,c5, a9 and the same bytes are received at the receiver end. The checker block compares all the bytes, since all the bytes match it outputs test passed.

```
rec_parity=a9 rec_paclen=7 , destination_address=81
[CHECKER] Checker started for pkt_no        0
[CHECKER] at         0 sentbyte 81 rcevbyte 81
[CHECKER] at         1 sentbyte 01 rcevbyte 01
[CHECKER] at         2 sentbyte 07 rcevbyte 07
[CHECKER] at         3 sentbyte 76 rcevbyte 76
[CHECKER] at         4 sentbyte 3d rcevbyte 3d
[CHECKER] at         5 sentbyte ed rcevbyte ed
[CHECKER] at         6 sentbyte 8c rcevbyte 8c
[CHECKER] at         7 sentbyte f9 rcevbyte f9
[CHECKER] at         8 sentbyte c6 rcevbyte c6
[CHECKER] at         9 sentbyte c5 rcevbyte c5
[CHECKER] at        10 sentbyte a9 rcevbyte a9
length =         7
ISim>
# run all
############## TEST PASSED ###############
```

Fig. 7 Checker output

## VII. CONCLUSIONS

We have presented an adaptive router design using buffer resizing technique for Network-on-chip (NOC).Buffer resizing technique with a floating FIFO is implemented in the router design to reduce the congestion of data packets which has positive effect on the speed. The basic elements of router such as FIFO, FSM controller and arbiter are designed and simulated using verilog HDL on Xilinx Isim simulator tool. With buffer resizing technique it is observed that, when static FIFO is full, floating FIFO is assigned to that particular port and the data is available at each clock cycle. Hence data congestion is reduced by employing the proposed buffer resizing technique. The design is verified by developing a verification environment in system verilog HVL using Questa SIM simulator tool. The verification components driver, receiver, scoreboard are developed in system verilog. RTL design and functional verification flow is studied and developed.

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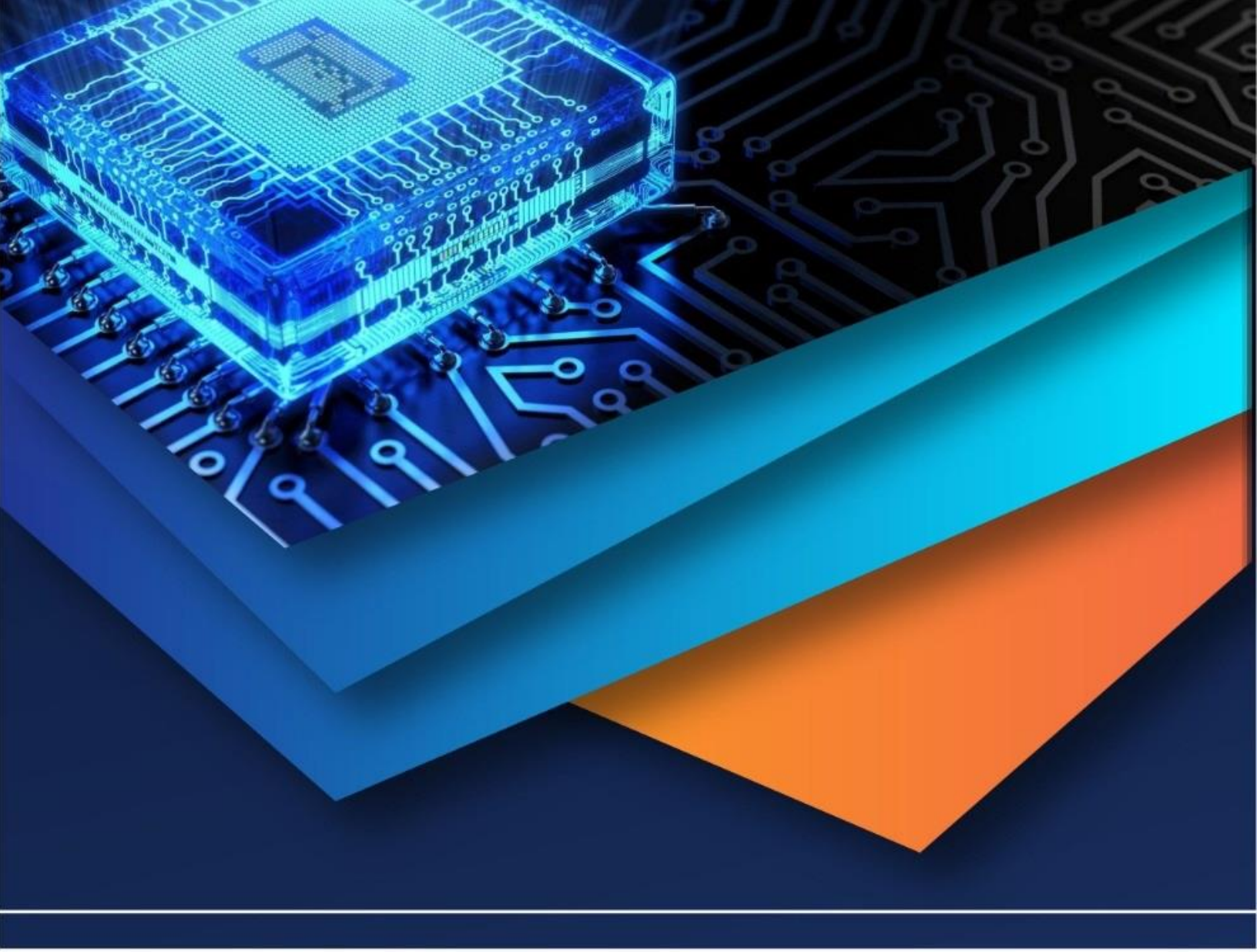

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