iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 4 **Issue:** VII **Month of publication:** July 2016

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

Volume 4 Issue VII, July 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Snubberless Soft-switching (zcs/zvs) Closed loop Current-fed Half-bridge Converter Based PV Inverter

Hemalata M Hiremath [1], T.N. Raghavendra[2]
Department of Electrical Engineering, Bengalore University, Bengalore.

Abstract: ***Snubber circuit dissipates some amount of the output power along with increase in circulating current through the components, increasing their conduction losses and also increases the components count, converter complexity hence the efficiency will reduce. This paper proposes snubberless soft switching (ZCS and ZVS) closed loop current fed half-bridge converter based inverter for photovoltaic applications. It is suitable for off-grid (standalone) as well as grid-tied (utility interface) application based on the mode of control. Proposed converter attains clamping of the device voltage by secondary modulation, thus eliminating the need of snubber. Zero-current switching (ZCS) or natural commutation of primary devices and zero-voltage switching (ZVS) of secondary devices is achieved. Soft switching is maintained during wide variation in voltage and power transfer capacity, Output voltage from PV is stabilized by the feedback loop and thus is suitable for PV applications. Primary switch voltage is clamped at reflected output voltage and secondary switch voltage is clamped at output voltage. Design and analysis of the operation are presented. Simulation results are obtained from MATLAB and compared the results with openloop. The proposed converter is a true isolated boost converter and has higher voltage conversion ratio compared to conventional active-clamped converter.***

Keywords: ZCS, ZVS, Front end DC-DC converter, Snubberless, PV Inverter, and Current fed.

I. INTRODUCTION

In developing countries and under developed countries, there is severe shortage of electrical energy. Because of the large gap between the demand and supply, the electric utilities will resort to frequent load shedding. Apart from this, sometimes it is not possible to take electric grid to remote areas because of the environmental and economical reasons. Under such conditions electrical energy can be generated from the alternative energy sources. One such alternative source of electric energy is solar energy.

But solar energy produces unregulated and discontinuous output and, therefore cannot be used in its original form. A power conditioner is essential to obtain a regulated stable output in useful form. Solar energy is integrated with energy storage to form a distributed generating system focusing on long term sustainability. Solar power generation using photovoltaic cell is a flexible power generation technique, which is scalable from small scale residential application to large scale solar power plants. Major disadvantage of this is high initial investment, which has been dropped significantly over past few years due to mass production and expected to be cheaper in future.

Power electronic inverters are essential in order to convert unregulated dc output from PV panel into useful ac form. Various frontend converter modules and inverter schemes have been introduced in literature [1] for single-phase PV inverter. Single-stage inverters are not preferred since it has low frequency transformer which is bulky, heavy, and costly. Present trend is to develop high-frequency (HF) transformer isolated multi-stage inverter topologies with either rectified sine link constant dc link or [2]. DC-to-DC converter is an electronic circuit which converts a source of direct current (DC) from one voltage level to another and inverter is controlling the output voltage, with a transformer we can achieve high efficiency voltage amplification.

Current-fed converter under input voltage control at PV side has less stability constraints than the voltage-fed converters [3-4]. Since at the input of PV current ripple swings the output power around the maximum power pint (MPP), this ripple has to limit in the safer zone. Current-fed converters not only helps in reduction of input current ripple, but also reduce the filter size across the PV strings. Current-fed converters also maintain high efficiency with wide variation in input (source) voltage and output power, which is a case in renewable energy sources.

The technique called soft-switching reduces the conduction losses even though increasing the switching frequency of semiconductor devices above 20 kHz till MHz range to realize a compact, light, and low cost converter. However, to retain soft-switching over a wide variation in source voltage and output power is a challenge [5]. Loss of soft-switching results in significantly very low

Volume 4 Issue VII, July 2016
ISSN: 2321-9653

efficiency which may occur typically in case when PV voltage changes with temperature and solar irradiance. A nearly flat efficiency curve is desired for better utilization. Recently isolated current-fed converters have been demonstrated and justified for such applications ,however, the major limitations of such converters is requirement of an active-clamp or passive snubber to absorb the switch turn-off voltage spike [6] to limit the device voltage. Active-clamp assists in ZVS of switches, but it dissipates around 2% of the output power along with increase in circulating current through the components, increasing their conduction losses, particularly at light load. Furthermore, it increases the components count and converter and control complexity also.

By the secondary modulation it is possible to divert the primary switch current into the transformer, causing transformer current to rise and the primary switch current to fall to zero naturally resulting in zero current turn off (ZCS) and clamping the voltage across the devices without any extra circuitry (snubber), where the active clamping or passive lossy snubbers are employed to limit the voltage spike across the switches at their turn-off. Here voltage is limited by secondary modulation without snubbers[7]. Secondary side switches undergo ZVS enhancing the converter performance hence efficiency of the system. Secondary modulation based naturally-clamped snubberless current-fed soft-switching half-bridge dc/dc converter as shown in Fig. 1. [7]

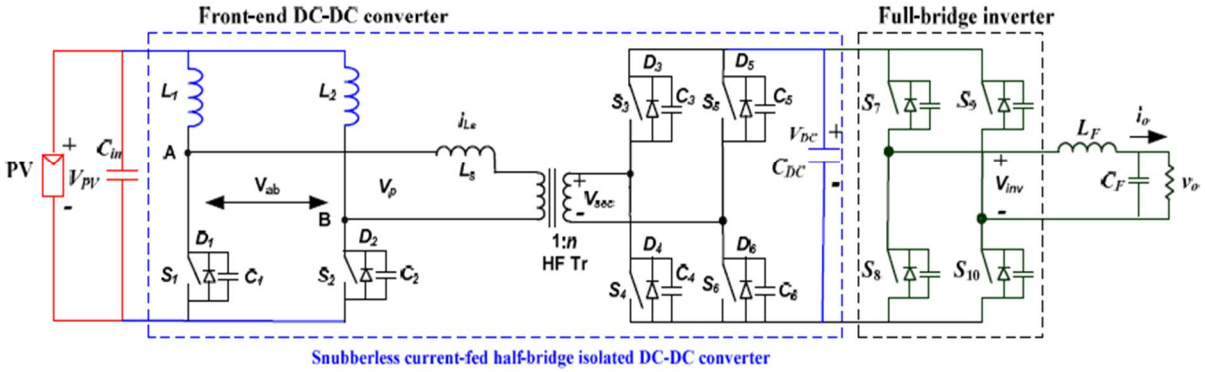


Fig. 1. Inverter with snubberless current-fed half-bridge dc/dc converter.

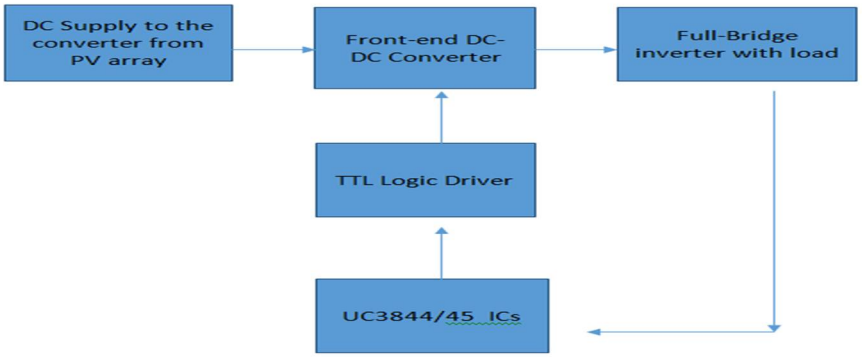


Fig.2. Block diagram of the complete proposed inverter

This paper proposed closed loop current fed soft switching half-bridge converter based inverter, the only disadvantage in the literature [1] is the output varies with respect to input to overcome this a feedback loop is used in this paper. In practice UC3844/45 IC is used. With this the output of the inverter is stabilized to a particular voltage for various applications, mainly in PV application. Fig. 2 Shows the block diagram of the complete proposed inverter, using simple TTL driver circuit to generate gate signals to the MOSFET switches. The UC3844, UC3845 series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components.

The objectives of this paper are: 1) to present the detailed steady-state operation and analysis with natural-clamping or zero-current-switching turn-off concept by secondary modulation (Section II), 2) to illustrate the design of the inverter (Section III), 3) to present and discuss simulation results using MATLAB13a to verify the analysis and design, and comparing the open loop and closed loop system performance to ensure the output voltage in closed loop stabilized to 200V and claimed natural commutation, soft-switching (ZCS of primary and ZVS of secondary devices) over wide voltage variations, snubberless clamping of devices (Section IV).

II. STEADY-STATE OPERATION AND ANALYSIS

Steady-state operation and analysis of the proposed inverter have been explained in this Section. Main focus is on the proposed front-end dc-dc converter. Current-fed front-end half-bridge converter is controlled using fixed-frequency duty cycle modulation. Before removing the gate signal from any one switch of the primary side to turn it off , other primary switch is turned-on. The reflected dc link voltage *VDC*/*n* appears across the transformer primary which intern across AB terminals shown in fig 1. If one switch is already conducting this reflected voltage appears across the other switch of the primary. The voltage across the transformer primary diverts the switch current into the transformer, causing transformer current to rise and the primary switch current to fall to zero. This current flows to the transformer through the body diode of the primary switch then the gating signal is removed causing its ZCS turn-off or natural commutation.

The following assumptions are made to understand and analyse the converter operation: 1) Inductors *L*1 and *L*2 are very large and maintain constant current through them. 2) Magnetizing inductance of the transformer is infinitely large. 3) *LS* is a series inductor that includes the transformer leakage inductance. 4) All the components are assumed ideal.

Primary side switches *S*1 and *S*2 are controlled by gating signals shifted in phase by 180º with an overlap in open loop [7].The overlap varies with duty cycle symbolized by *D*, which is always greater than 50%, in this paper its from 60-80%. The converter operation during different intervals in a half HF cycle is explained by equivalent circuits shown in Fig.3.

Mode 1 (Fig. 3a; to < t < t1): In this interval, primary side switch *S*1 and anti-parallel body diodes *D*4 and *D*5 of secondary side switches S_4 and S_5 respectively are conducting. Power is fed through the HF transformer to the inverter from the source. Current through series inductance L_s is negative and constant. Switch S1 carries the entire input current. The values are *iS*1 = *Iin*. *iS*2 = 0, *iLs* = -*Iin*/2, *iD*4 = *Iin*/2*n*, *VS*2 = *V*DC/*n*.

Mode 2 (Fig. 3b; t1 < t < t2): In this interval, device capacitance across the device *S*2 discharges quickly . Switch *S*2 is tending to turned on. It is a very short interval.

$$i_{D4} = \frac{I_{in}}{2n} - \frac{V_{DC}}{n^2 \cdot L_s} \quad (1)$$

At the end of this interval *t* = *t*3, switch current *iS*1 reduces to half of the input current *Iin*/2 and half will flow through switch *S*2 , series inductor current *iLs* reaches zero, and secondary switch/diode current reduces.

Mode 3 (Fig. 3c; t2 < t < t3): In this interval, switch *S*2 of primary side starts conducting. series inductor current *iLs* , becomes positive hence it starts transferring the current to switch *S*2 with a slope limited by *LS*. The current is a ramp, starts from zero, resulting zero current turn-on of the switch *S*2. It reduces conduction losses or losses associated with turn-on process of primary switch S2. The current through the the series inductor Ls, switch currents *S*1 ,*S*2 respectively are given by

$$i_{Ls} = -\frac{i_{in}}{2} + \frac{V_{DC}}{L_s n}(t - \quad (2)$$

$$i_{s1} = i_{in} - \frac{V_{DC}}{L_s n}(t - \quad (3)$$

$$i_{S2} = \frac{V_{DC}}{n \cdot L_s}(t - \quad (4)$$

At the end of this interval *t* = *t*4, the switch current *iS*1 naturally tending to zero attaining zero-current switching turn-off. Final values of the different components are: *iS*2 = *Iin*, *iS*1 = 0, *iLs* = *Iin*/2, *iS*4 = *Iin*/*n*.

Mode 4 (Fig. 3d; t3 < t < t4): In this interval, secondary switches *S*4 and *S*5 are turned-on with ZVS.

Mode 5 (Fig. 3e; t4 < t < t5): During this interval, the anti parallel body diode *D*1 of switch *S*1 starts conducting causing zero voltage across the switch *S*1 ensuring its ZCS. Switch current *iS*2 and series inductance current *iLs* reach their peak values. This interval should be very short in order to limit the peak current through the components and to reduce the current stress and hence kVA rating. The current through the components are given by

$$i_{Ls} = \frac{I_{in}}{2} - \frac{V_{DC}}{n \cdot L_s}(\quad (5)$$

Volume 4 Issue VII, July 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

$$i_{S2} = I_{in} - \frac{V_{DC}}{n \cdot L_S}(\quad (6)$$

This is a diode conduction interval and very short, and is kept to ensure ZCS of primary side devices .

Mode 6 (Fig. 3f; t5 < t < t6): In this interval, secondary switches *S*4 and *S*5 are turned-off. Other pair of body diodes of the secondary switches *S*3 and *S*6 take over the current immediately. The currents are given by

$$i_{Ls} = I_{Ls,peak} - \frac{V_{DC}}{n \cdot L_S} \quad (7)$$

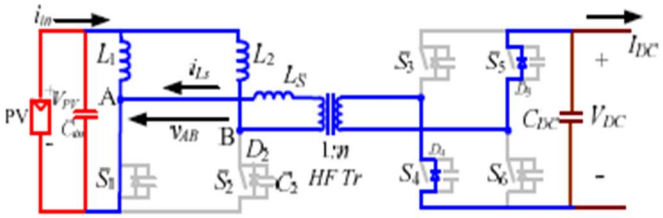
$$i_{S2} = I_{S2,peak} - \frac{V_{DC}}{n \cdot L_S} \quad (8)$$

The peak currents through switch *S*2 and inductance *LS* decrease to value same as final values of interval 4. Body diode *D*1 of switch *S*1 commutates at the end of this interval. Final values are: *iS*2 = *Iin*, *iD*1 = 0, *iLs* = *Iin*/2, *iS*4 = *Iin*/2*n*.

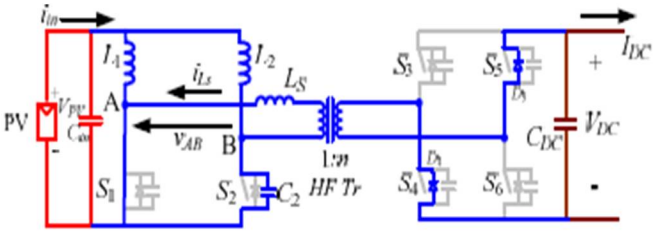
Mode 7 (Fig. 3g; t6 < t < t7): In this interval, the switch *S*1 getting into forward blocking mode device capacitance charges to *V*DC/*n*. This interval is very short.

Mode 8 (Fig. 3h; t7 < t < t8): In this interval, current through switch *S*2, series inductance *LS* and body diode of secondary switch is constant.

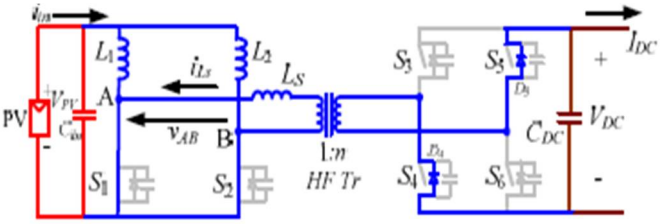
Half HF switching cycle ends here with the end of this interval. The intervals are repeated for the next half cycle, in the same sequence .



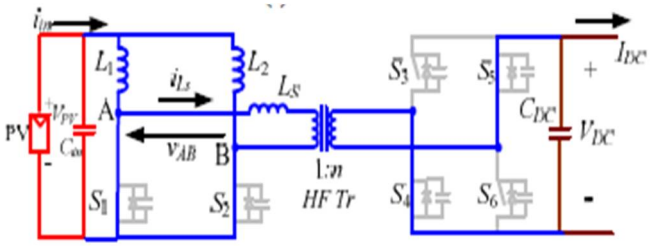
(a) Mode 1



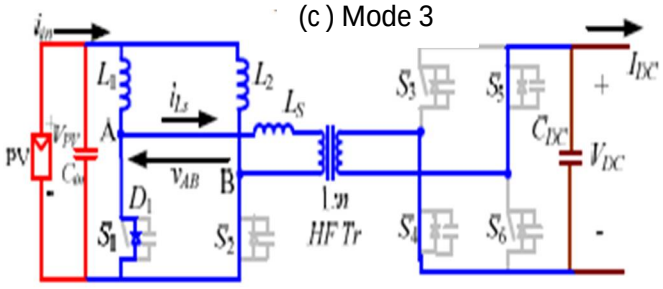
(b) Mode 2



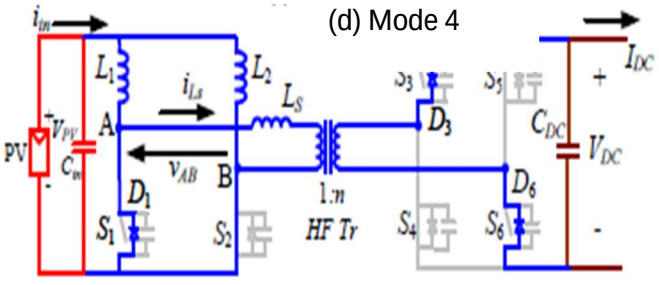
(c) Mode 3



(d) Mode 4

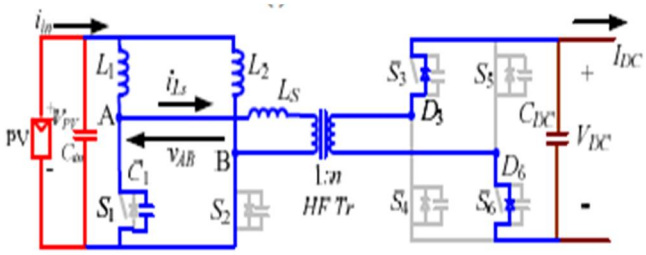


(e) Mode 5

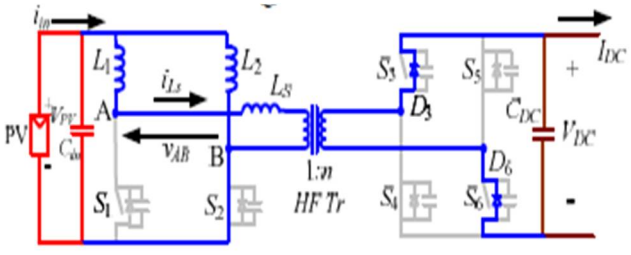


(f) Mode 6

Volume 4 Issue VII, July 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)



(g) Mode 7



(h) Mode 8

Fig .3 Equivalent circuits during different intervals of the operation of the proposed converter

Full-bridge inverter is to produce useful ac voltage from the dc link. Inverter devices are controlled by standard sine pulse width modulation (SPWM). In SPWM either unipolar or bipolar PWM with fixed-frequency modulation can be used to obtain ac output voltage at utility line frequency.

III. INVERTER DESIGN

In this Section, design procedure for the following converter has been given.

TABLE.1
SYSTEM SPECIFICATIONS

maximum open circuit voltage of PV *Voc,max*	50V
voltage of PV panel at MPP *VPV*	25V to 41V
maximum current at MPP *Iin*	9A
peak output power *P*o	200W
voltage at DC link *V*DC	200V
output voltage *V*o	110V rms
device switching frequency of dc/dc converter *fs*	100kHz
switching frequency of inverter *fsi*	20kHz

A. Average input current is $I_{in} = \frac{P_o}{V_{PV}n}$ Assuming an inverter efficiency nearly 95%, Iin = 9.6 A.

B. Maximum voltage across the primary switches is $V_{s1,sw} = \frac{V_{DC}}{n}$ (9)

Where n is the transformer turns ratio considered as n= 2

C. Voltage conversion ratio or input and output voltages of the converter are related as $V_{PV} = \frac{(1-D).V_{DC}}{n}$ (10)

For *D* = 0.8, the proposed converter can boost up to 5 times.

Output current of the converter *IDC* is given by (11), where *Iin* is the output current from the PV module obtained depending on the PV characteristic, solar irradiance and temperature. $I_{DC} = \frac{(1-D).i_{in}}{n}$ (11)

D. *Series inductance LS is given as* $L_s = \frac{V_{DC}\,(D-.5)}{I_{in}\,f_s\,n}$ *(12)*

E. *RMS current through the primary switches is given by* $I_{s1,rms} = I_{in}\sqrt{\frac{2-D}{3}}$ *(13)*

The calculated value is *IS*1, *rms* = 6.1 A.

This expression is derived assuming that anti-parallel diode conduction time is very small and insignificant as it is desired simply to ensure ZCS and to reduce the device peak currents.

Transformer turns ratio n is selected based on the conduction losses in the system or in other words the converter efficiency, which mainly depends upon the losses in primary switches because they carry higher currents compared to other devices. Transformer with

higher turns ratio requires low voltage switches (using (7)), which have low on-state resistance. On the contrary, higher turns ratio results in higher switch RMS current (using (11)). Therefore, an optimum turns ratio, and duty cycle, resulting in minimum conduction loss of primary switches needs to be selected. Turns ratio of n = 2, duty ratio D = 0.8 results in overall low conduction losses. Output voltage from PV module can be varied from 22V to 41V by varying the duty ratio from 0.8 to 0.6. From (10), series inductance LS = 31.25 µH for the given values.

F. RMS current through the primary winding of the transformer is given by $I_{Ls,rms} = I_{in}\sqrt{\frac{5-4D}{12}}$ (14)

The calculated value is ILs, rms = 3.7 A.

G. Values of boost inductors are given by $L_1 = L_2 = \frac{V_{PV} \cdot D}{\Delta I_{in} \cdot f_s}$ (15)

Where Δ*Iin* is the boost inductor ripple current.

For Δ*Iin* = 0.5 A, *L*1 = *L*2 = 352 μH. Each boost inductor has average current rating of *Iin*/2 (= 4.8 A).

Currents through boost inductors *iL*1 and *iL*2 are phase shifted by 180º and results in smaller ripple magnitude in source current.

H. Average current through secondary devices is given by *IS*3, *av* = *Po* / (2*VDC*) (16)

Here, *IS*3, *av* = 0.5 A. Voltage rating of secondary side devices = *VDC* = 200 V.

I. RMS current through the secondary side switches is given by

$$I_{s3,rms} = \frac{I_{in}}{2.n}\sqrt{\frac{5-4D}{6}} \quad (17)$$

Peak current through the secondary switches is $I_{s3,peak} = \frac{I_{in}}{2.n}$ (19)

The calculated value *IS*3, *rms* = 1.6 A.

J. VA rating of HF transformer is given by $VA_{x-mer} = \frac{V_{DC} \cdot I_{in}}{n}\sqrt{\frac{(5-4D).(1-D)}{6}}$ (20)

The calculated value is *VAX-mer* = 235 VA.

K. DC link capacitor C_{DC} is $C_{DC} = \frac{I_{in}}{2.n.\Delta V_{DC}.f_s}(D - .5)$ (21)

Δ*VDC is* the allowable ripple in output voltage. *CDC* = 14.4 µF for Δ*VDC* = 0.5 V. Switches have to be rated for DC link voltage i.e. 200V.

L. Average current through the full bridge inverter switches is given by $I_{s7,avg} = \frac{\sqrt{2}P_0}{V_0\pi}$ (22)

Peak current through the inverter switches is $I_{s7,peak} = \frac{\sqrt{2}P_0}{V_0}$ (23)

The values of the same are obtained as *IS*7, *avg* = 0.82A and *IS*7, *peak* = 2.6A. Its voltage rating is equal to *VDC* = 200 V.

M. Filter inductor is calculated to keep the voltage drop across it less than 2% of the nominal voltage.

$$L_F = \frac{0.02V_0}{2\pi.f_0.I_0} \quad (24)$$

Where, *Io* and *fo* are the output current and output frequency. The value *LF* is obtained as 3.8mH.

Filter capacitor is decided according to the cut-off frequency of the low pass filter. For this application, one tenth of inverter switching frequency *fsi* is selected as the cut-off frequency. Capacitor is calculated as, $C_F = \frac{1}{4\pi^2 f_c{}^2 L_F}$ (25)

IV. SIMULATION RESULTS

In this paper the designed converter rated at 200W was first simulated using MATLAB13a for open loop then after with the closed

Volume 4 Issue VII, July 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

loop to verify the proposed analysis and design and to compare the results with closed loop simulation to ensure the stabilization of the system voltage. Solar irradiance (Power per unit area received from the sun) is considered as 25, 600 and 1000W/m^2. With respect to these values PV array will generate the DC voltages 25, 35 and 42V in steps of 0.05sec. With these input voltages proposed Half bridge DC-DC converter generates output. Output of the inverter is considered as the Input of the single stage inverter.

Fig. 4(a) shows the open loop simulation circuit. Fig. 4(b) shows the pulses for the converter switches. Fig. 4(c) shows the input voltages to the converter from the PV panel. Fig. 4.(d) shows transformer current *iLs* and voltage, switch currents *iS*1 and *iS*2 through primary switches *S*1 and *S*2 and secondary switch currents through (*S*3, *S*6), (*S*4, *S*5) Fig 4.(e) shows the DC link voltage and output current of the converter. Fig 4(f) shows the final output of the inverter using low pass filter circuit.

Fig. 4(d) clearly shows ZCS turn off of primary switches, where current reaches zero naturally and anti-parallel body diode of the device starts conducting before gate signal is removed. This naturally clamps the switch voltage without any additional snubber. It is clear from *iS*3 and *iS*4 in Fig. 4(d) that the body diode of the secondary switches *S*3 and *S*4 conduct before the switches start conducting. It results in their ZVS turn-on.

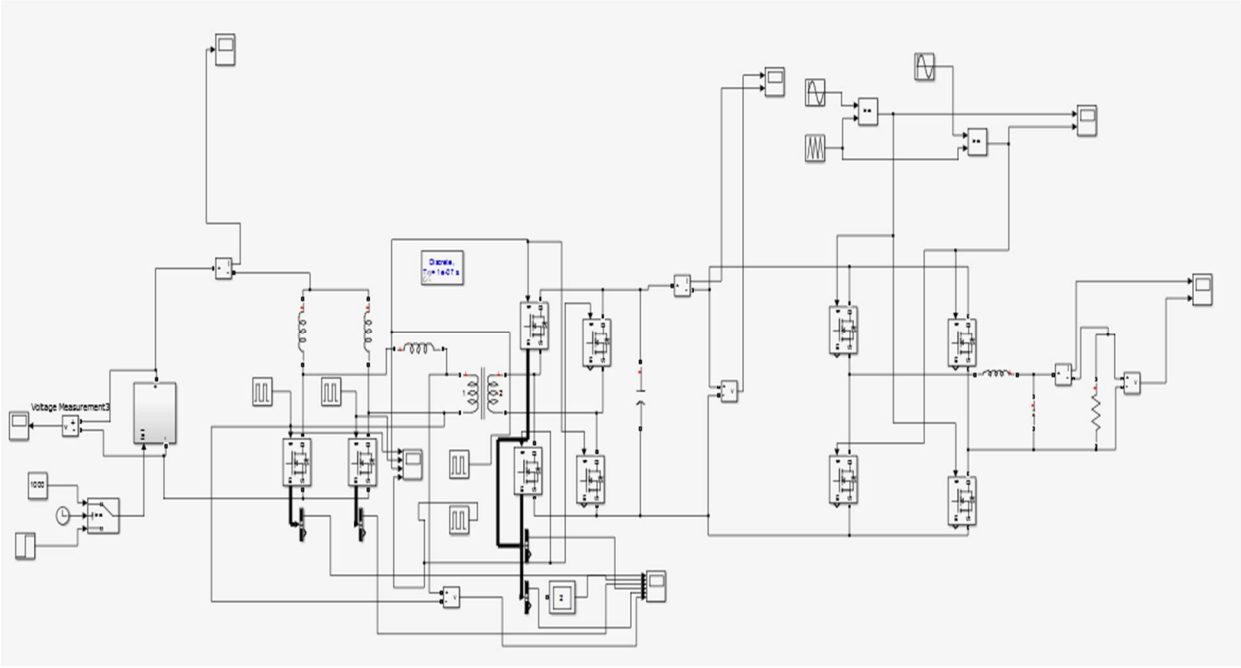


Fig. 4(a) shows the open loop simulation circuit.

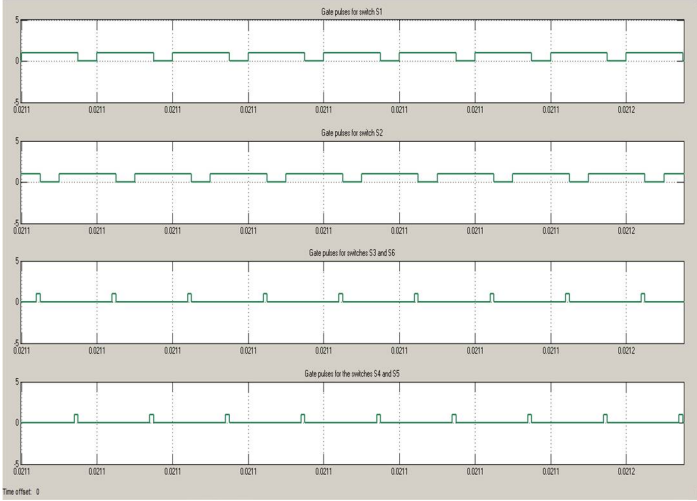


Fig. 4(b) Pulses for the converter switches.

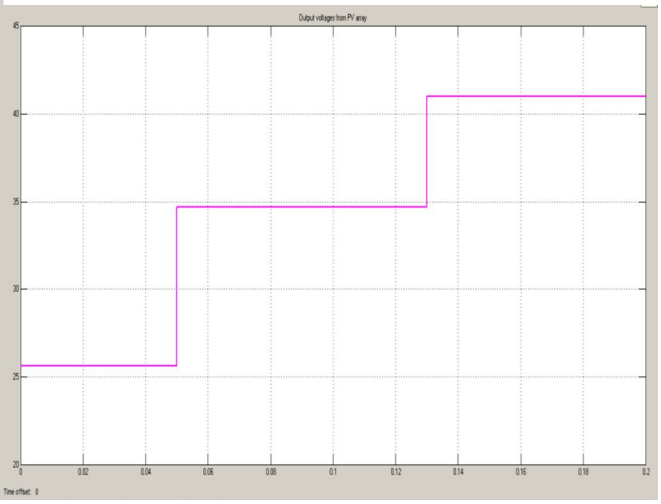


Fig. 4(c) Input voltages to the converter from the PV panel.

Volume 4 Issue VII, July 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

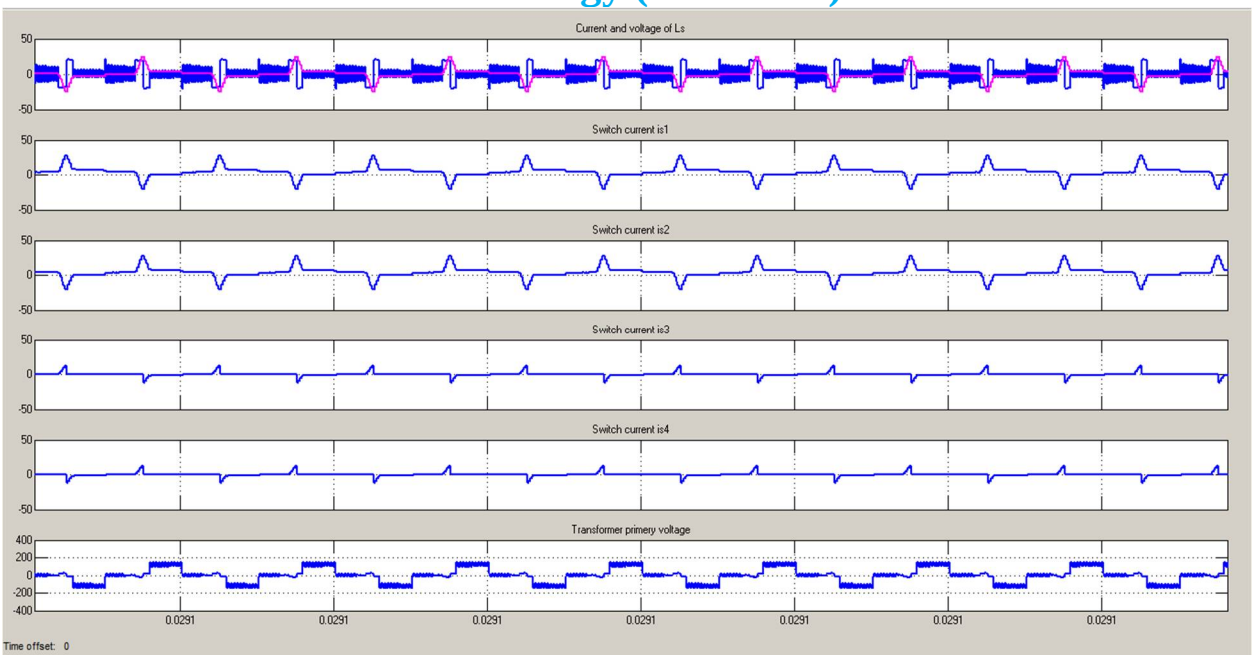


Fig. 4.(d) Current and voltage of the series inductor Ls, switch currents *iS*1 and *iS*2 through primary switches *S*1 and *S*2 and secondary switch currents through (*S*3, *S*6) , (*S*4, *S*5)

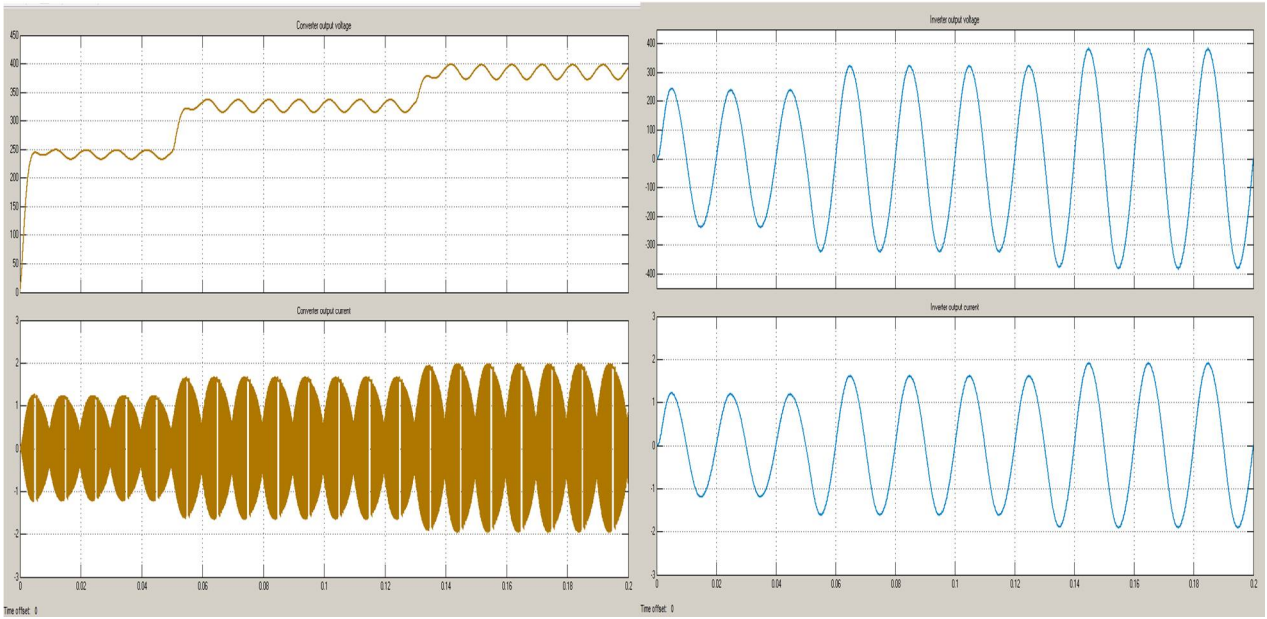


Fig. 4(e) DC link voltage and output current of the converter.

Fig. 4(f) Final output of the inverter

Fig. 5(a) shows the closed loop simulation circuit. Fig. 5(b) shows the current control feedback loop in simulation with reference voltage as 200V. Fig.5 (c) shows the step response of the PI controller in MATLAB.Fig. 5(d) shows the pulses for the converter switches. Fig. 5(e) shows the input voltages to the converter from the PV panel. Fig. 5(f) shows transformer current *iLs* and voltage, switch currents *iS*1 and *iS*2 through primary switches *S*1 and *S*2 and secondary switch currents through (*S*3, *S*6), (*S*4, *S*5) Fig. 5(g) shows the DC link voltage and output current of the converter. Fig. 5(h) shows the final output of the inverter using low pass filter circuit.

Volume 4 Issue VII, July 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

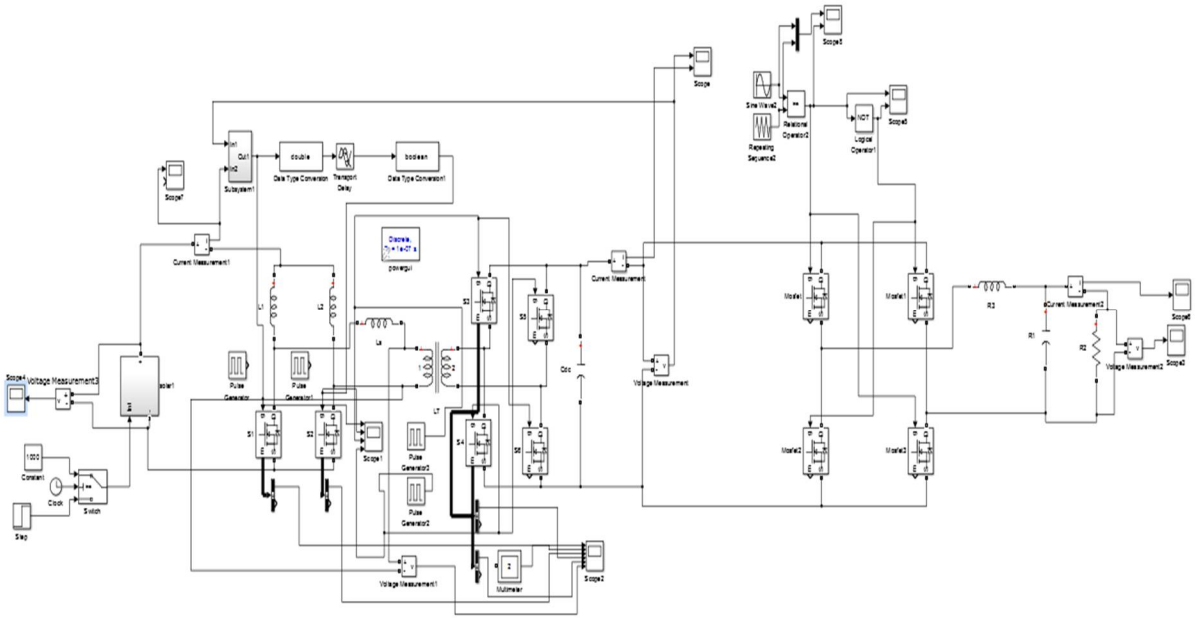


Fig. 5(a) shows the closed loop simulation circuit.

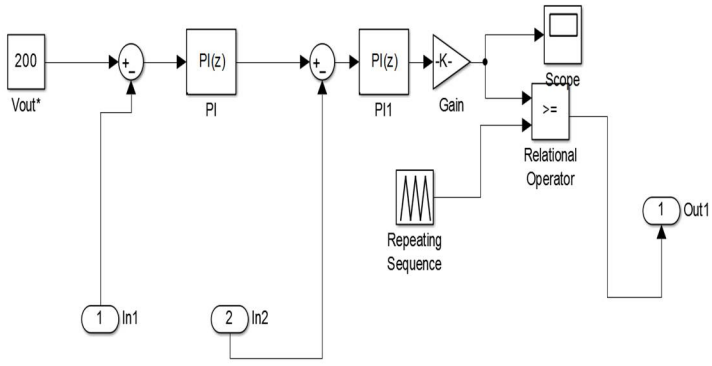


Fig. 5(b) Simulation model of current control feedback loop

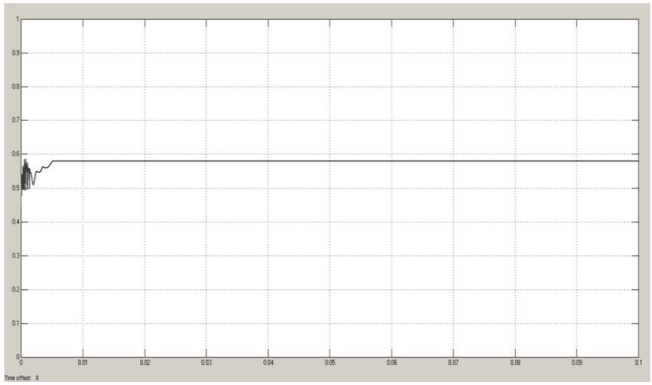


Fig. 5(c) Step response of the PI controller

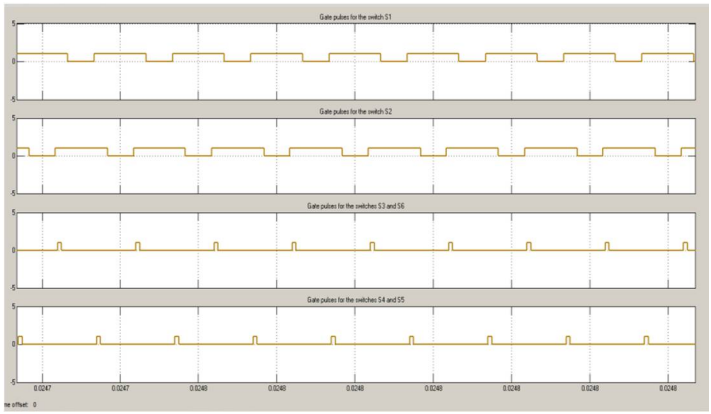


Fig. 5(d) Pulses for the converter switches.

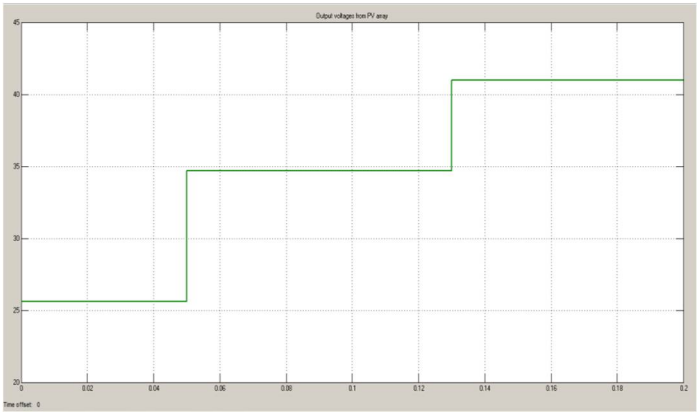
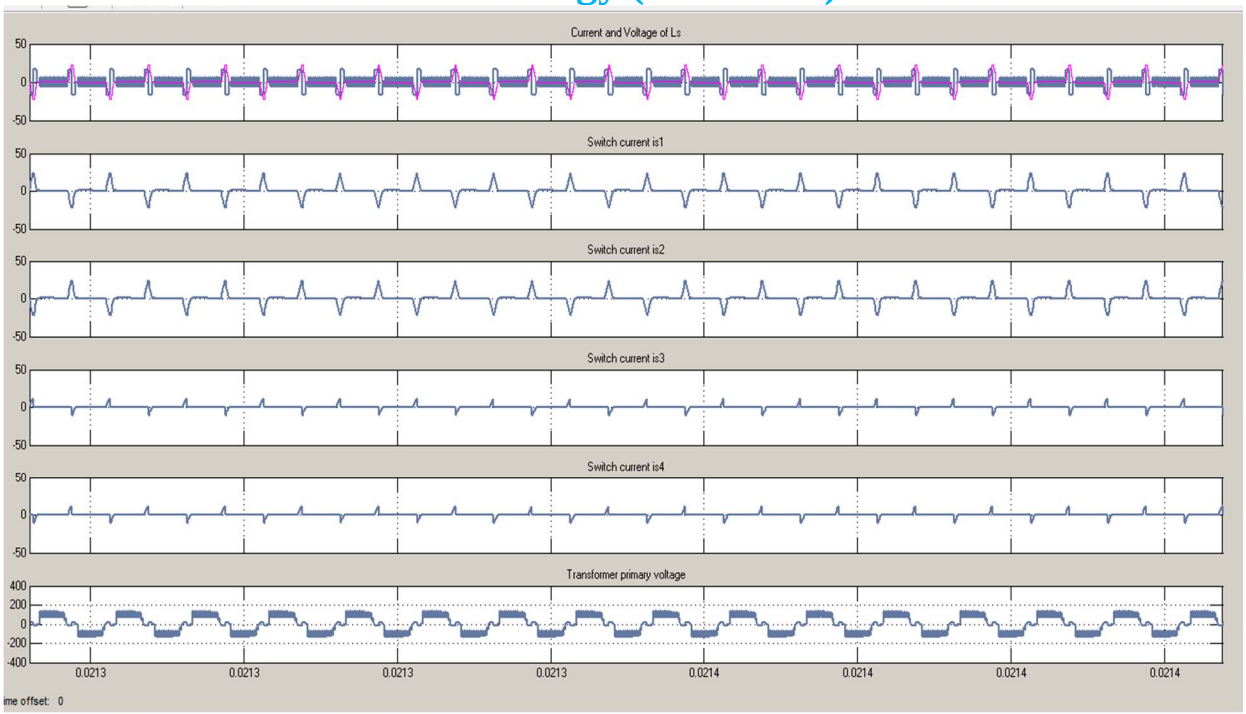


Fig. 5(e) Input voltages to the converter from the PV panel

Volume 4 Issue VII, July 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)



5.(f) current *iLs* and voltage of the series inductor Ls, switch currents *iS*1 and *iS*2 through primary switches *S*1 and *S*2 and secondary switch currents through (*S*3, *S*6), (*S*4, *S*5)

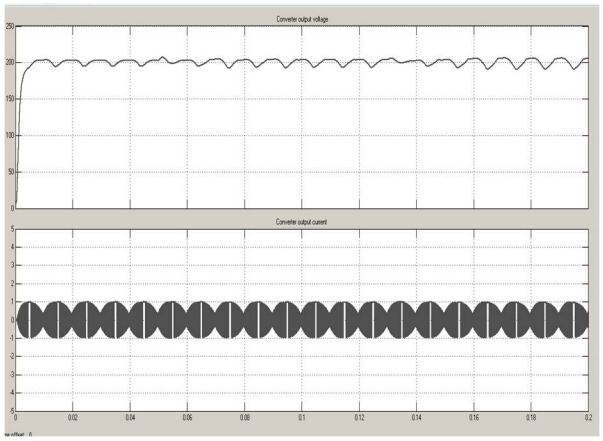


Fig 5.(g) DC link voltage and output current of the converter

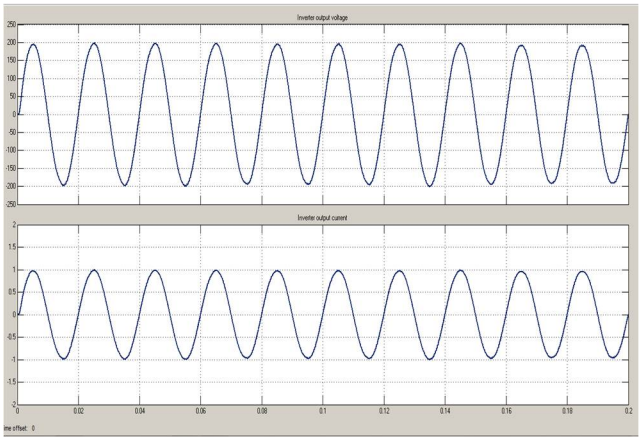


Fig 5(h) shows the final output of the inverter

A. How to tune the PI-controller

There are more ways to tune the PI-controller, a simple rule is:

1) Turn OFF the integration part of the controller.
2) Try to tune in the proportional gain, Kp, until the result is OK.
3) If 2) do not accomplish your control target, then turn ON the integrator part by reducing Kp to the half of what you have already found and then turn slowly.

From Fig. 4(e) and 5(g) it is clear that with the closed loop (feedback control loop) the solar irradiance can be stabilized to a particular voltage and this controlled voltage is fed to the full bridge inverter to convert and control the useful AC form, it can be shown from the fig 5.(h). THD of both open loop and closed loop inverters are shown in fig. 6(a) and 6(b) respectively. With the open loop THD of the inverter voltage signal is 1.82% and with closed loop it is 1.35%

Volume 4 Issue VII, July 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

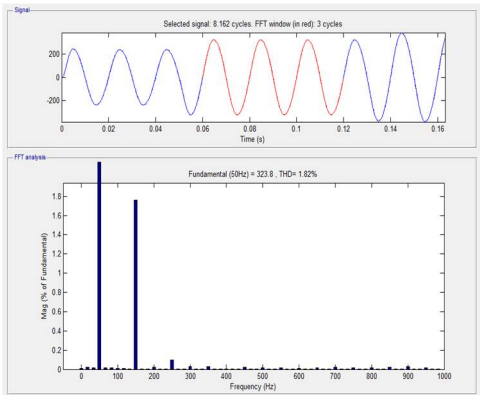


Fig. 6(a) THD of open loop inverter voltage

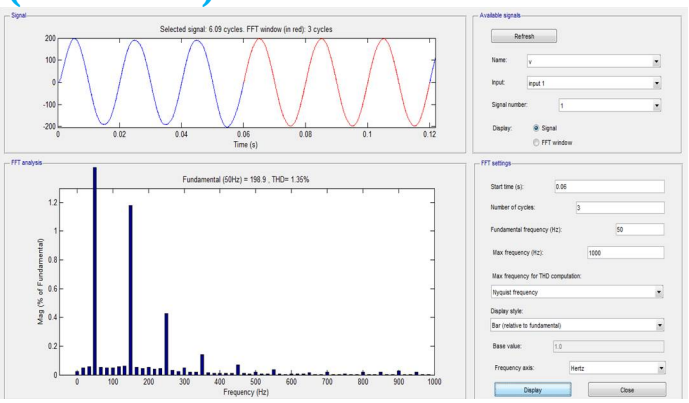


Fig. 6(b) THD of closed loop inverter voltage

V. CONCLUSION

Snubberless closed loop current fed soft switching half bridge converter based inverter has been presented in this paper. Openloop and closed loop system results are compared. Output of the PV inverter has been stabilized with the current controlled feedback loop. Efficiency of the inverter system is increased by using soft switching and secondary modulation techniques.

REFERENCES

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, “A review of single-phase grid-connected inverters for photovoltaic modules”, IEEE Trans on Industry Applications, vol. 41, no. 5, pp. 1292-1306, Sept./Oct. 2005.

[2] Z. Zhao, M. Xu, Q. Chen, J-S. Lai and Y. Cho, “Derivation, analysis, and implementation of a boost-buck converter-based high-efficiency PV inverter”, IEEE Transactions on Power Electronics, vol.27, no. 3, pp 1304-1313, Mar. 2012.

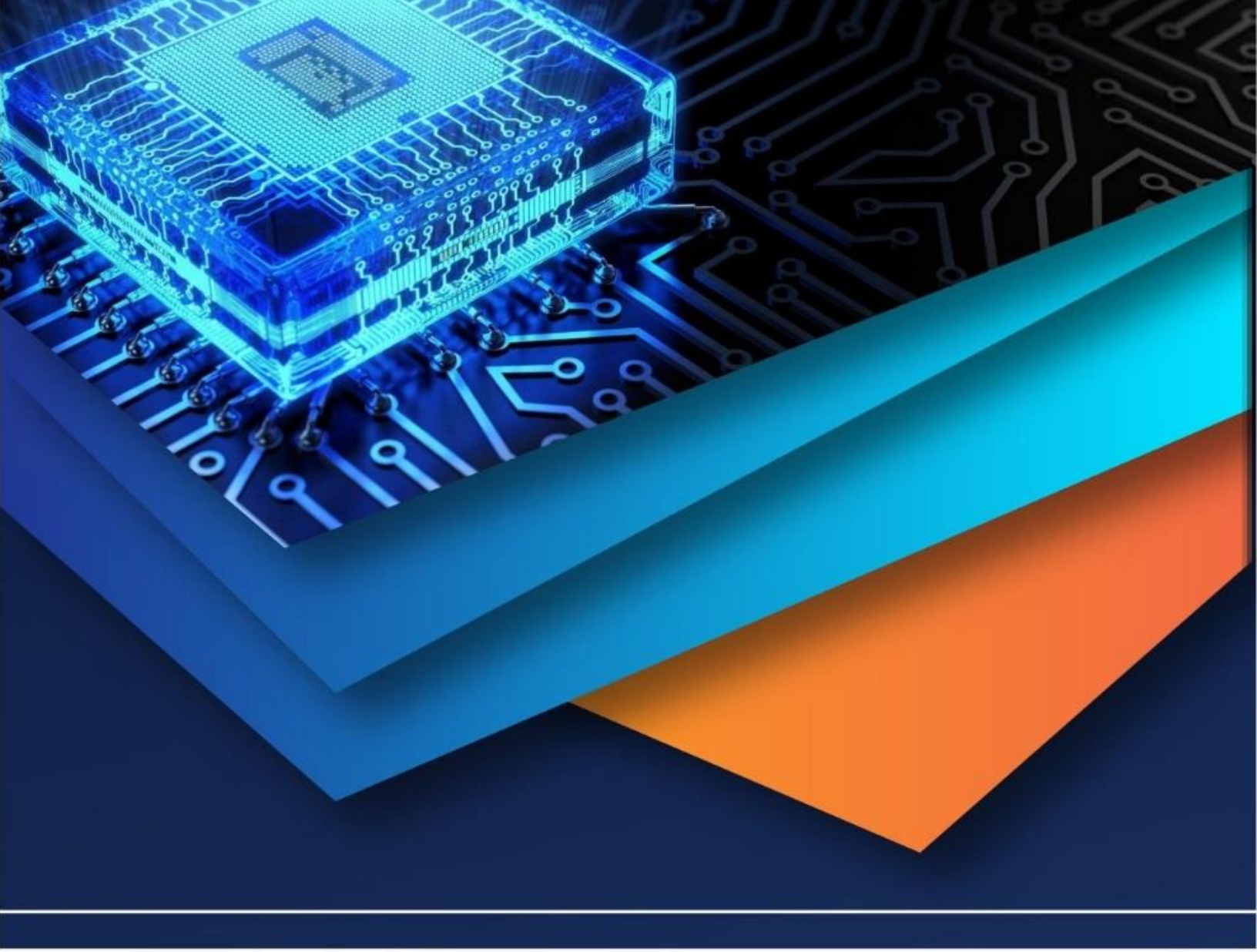
[3] T. Suntio, J. Leppaaho, J. Huusari, and L. Nousiainen, “Issues on solargenerator interfacing with current-fed mpp-tracking converters”, IEEETransactions on Power Electronics, vol. 25, pp 2409-2419, Sept. 2010.

[4] T. Suntio, J. Leppaaho, and J. Huusari, “Issues on solar-generator interfacing with voltage-fed converter,” in Proc. IEEE IECON, 2009, pp. 600–605.

[5] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, “A comparison of softswitched DC-DC converters for fuel cell to utility interface application’, IEEJ Transactions on Industry Applications, vol. 128, no. 4, pp. 450-458, 2008.

[6] S. J. Jang, C. Y. Won, B. K. Lee and J. Hur, “Fuel cell generation system with a new active clamping current-fed half-bridge converter,” IEEE Transactions on Energy Conversion, vol. 22, pp. 332-340, 2007.

[7] Udupi R. Prasanna, and Akshay K. Rathore, “Novel Soft-switching Snubberless Current-fed Halfbridge Front-end Converter Based PV Inverter”, IEEE Trans on Power Electronics, pp 4673-4355-8/13, 2013.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY