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Design of Pseudorandom Pattern Generator for MIHST

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Abstract -: The paper describes a system generator which produces Pseudo random sequence with user defined toggling range. The patterns were generated using PRPG; Detection of errors is done using Microprocessor Hardware Self Test (MIHST) for each pattern produced by generator. The MIHST is a permutation of BIST and SBST principles. A method is introduced for mechanical selection of some control signals of generator offering simple and exact tuning. The main intend is that due to PRESTO (pre-selected toggling level) switching activity for the period of scan loading is reduced. Using Micro processor hardware self test unit processor executes compact test sequences like SBST. Microprocessor Hardware Self Test is mainly used for processors online test rooted on system-on-chip, it overcomes limitations of SBST. The major benefit of MIHST is it utilizes less resources compared to SBST. The MIHST reduces time essential for the execution by removing instructions necessary for the test flow management.

Keywords: Built-in self-test (BIST), low-power (LP) test, pseudorandom test pattern generators (PRPG), SBST.

I. INTRODUCTION

In future, the most crucial target of test assembling will stay same, basically to guarantee solid and high element semiconductor item conditions furthermore critical movement has been experienced by test arrangements. The design procedure, semiconductor technology and design characteristics are the key in components which will affect this development. Decade back test compression techniques were introduced, which has become quickly the core stream of Design for Test methodology. LBIST (logic-built-in-self-test) created for framework, board and test field is ahead of time for test generation as it will give exceptionally powerful Outline to Test and it has been used gradually more with test compression. Preserving all scan firmness and LBIST advantages, it can diminish the manufacturing cost of test.

The variety of schemes used to decrease power through scan testing proposed. There are various arrangements purposely projected for BIST, to maintain the peak power and average beneath given limit. For instance, the power used during test is decreased by preventing transitions at recollection elements. This will be generated by adding up gating logic in between logic driven by them and scan cell results.

A burst clock controller backs off a portion of the movement cycles to diminish the voltage hang identified with a higher circuit action. It allows steady increase of circuit activity, in this manner decreasing di/dt effect. Depending upon the requirements for bit by bit warming of circuit shift clocks were gated by controller.

II. RELATED WORK

Michal Filipek proposed the work on preselected toggling sequence generation using LFSR, it shows test compression technique by which accurate and predictable result will be obtained. Generated sequence includes toggling levels of user distinct. The main intend is that due to PRESTO (pre-selected toggling level) switching activity for the period of scan loading is reduced [1].S. Bhunia proposes new circuit so power dissipation during testing is reduced; this is obtained at input level of logic circuit by signal alteration masking. Addition of extra one transistor in logic circuit results advantages in the field of area, power and delay fields [2] H. Mahmodi proposed the implementation of masking effect by addition of supply gating in the path from supply to ground, at flip-flop output [2]. E. G. McCluskey proposed method fault coverage perfection for test per each scan, BIST is used for test circuit modification by adding test points or the redesigning of circuit is done. Bit fixing sequence generator architecture is designed by him, architecture is designed to change bits of pseudorandom sequence shifted to scan chain for the addition of test cubes into sequence [4].

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Patrick Girard proposed a technique, i.e. irregular one information change test creation, which produces test succession of low power, so during circuit testing fault coverage at high level is achieved. Christian Landrault proposes equivalent BIST execution of RSIC producer and surveys the region overhead effect [8].

In this paper we are using MIHST for testing purpose, MIHST is Micro processor hardware built in self test. It is a permutation of BIST and SBST principles, by using Micro processor Hardware self test unit the processor execute the compact SBST test sequences. The main advantages of MIHST are, it decreases execution time for test, it better preserves the intellectual property of core processor and memory structure is not obligatory to neither preserve the test sequences nor test memory.

III. PROPOSED WORK

In this section will see the design of each block. The proposed method describe about the generation of patterns using PRESTO (Pre selected toggling level) and testing the device for each pattern generated by using microprocessor Hardware self test.

A. Test Design

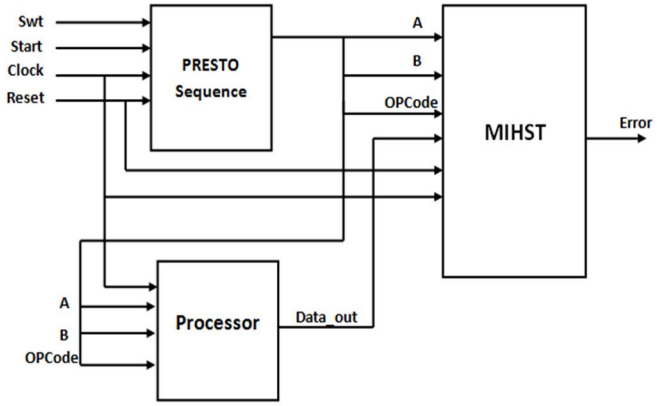

Fig -1: Test design

The test design consists of PRESTO, MIHST and Processor

Fig-1 shows test design block diagram, designed to test the processor for every sequence generated by PRESTO using MIHST the fault will be detected. The 32-bit preselected sequence is generated using PRPG.PRPG is designed using LFSR. The patterns generated by PRESTO consist of user distinct toggling rate. PRESTO pattern is given as input to MIHST test unit; processor performs operation to which it is designed for each sequence generated by PRESTO.

The 32-bit sequence from PRESTO is divided into two 8-bit inputs A and B and five bit OPCode. Using A, B and OPCode processor performs operation and processor output is given to MIHST. Test unit performs the operation like And, OR and rotate etc operations, check unit in MIHST detects fault present in processor by comparing output from processor and test unit.

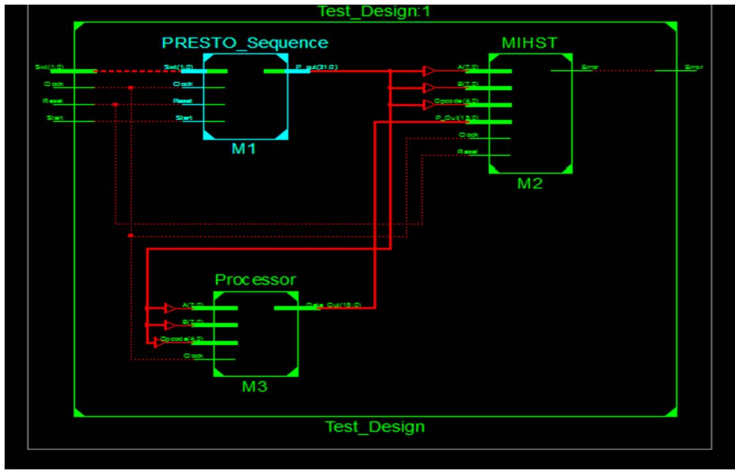

Fig-2: Test design RTL schematic

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B. Presto Generator Basic Architecture

The PRESTO structure consist of PRPG, Shift register, Phase shifter, switching circuit

Fig-3 shows the PRESTO Generator basic architecture. Phase shifter will be connected to the PRPG by supplying scan chains, pseudorandom patterns are produced.

The n numbers of hold latches are located between phase shifter and PRPG. Every hold latch is separately controlled by equivalent stage of n-bit control register. When latch is enable data to the phase shifter will be given from scan chains, if latches are disabled data to phase shifter will be given from PRPG.

Loading the scan string with low transitions count patterns are not only allowed by PRESTO generator thus drastically reduces power dissipation, along with it enables the selections of its control such that generated test sequence consist of user distinct toggling rates.

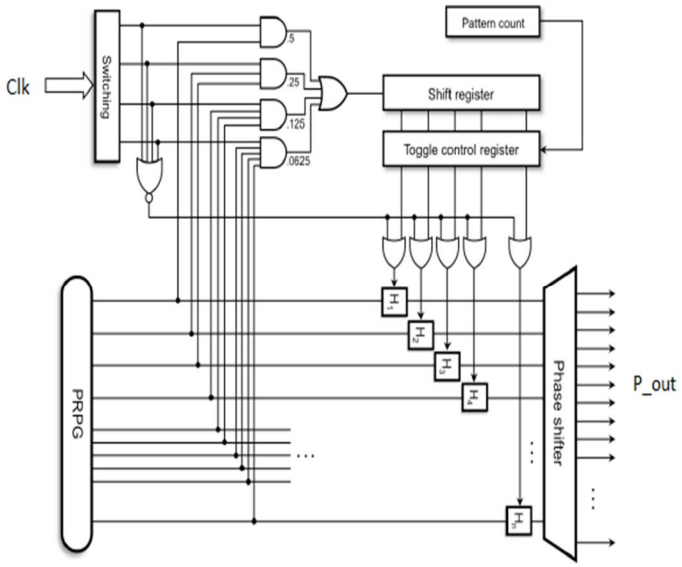

Fig-3: PRESTO Structure

For each pattern the reloading of control register is done by using the substance of shift register. The enable signals which are given to shift register be produced within probabilistic manner using PRPG which is original with programmable sets of weight.

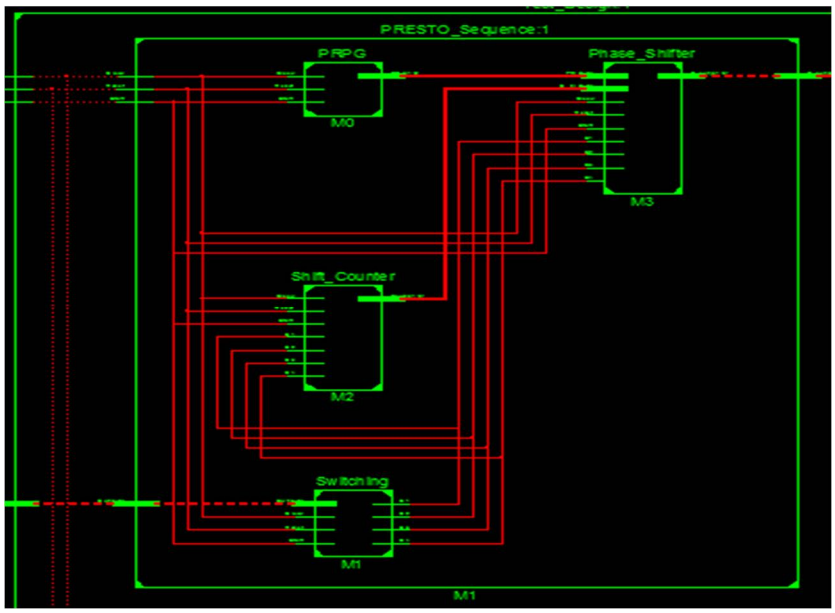

Fig-4: PRESTO RTL Schematic

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C. MIHST Architecture

Microprocessor Hardware Self Test is mainly used for processors online test rooted on system-on-chip, it overcomes limitations of SBST. This existing method adds significant features of functional based as well as Hardware based techniques.
MIHST Method exists on two thoughts

1) The device executes in two states one is normal state another is test state. When the device is in normal state, the processor runs commands which are translated from code memory. When test state exists the device runs the commands from MIHST unit.
2) The MIHST element encodes program which is to be tested internally in convention manner which shows the regularity of test program, hardware required for storage of test program is reduced.

By the result of above thoughts the processor runs commands from MIHST element but it will not control flow of execution.
This operational principle is critical because

1) When manipulating test program the collection of address will be manipulated by test engineer.
2) This allows monitoring the execution of instruction on bus without completing test procedure which is caused by faults.

The main benefit of MIHST is it utilizes less resources compared to SBST, as data and test code is stored in system memory. The MIHST reduces time required for the execution by removing instructions required for the test flow management.
MIHST unit will be programmed by extremely encoded data which is hardwired within it or uploaded by outside, in each case MIHST has advantages over SBST in case of IP protection, core users will not provided by test program. Thus architectural design of unit will be easily understood by test unit.

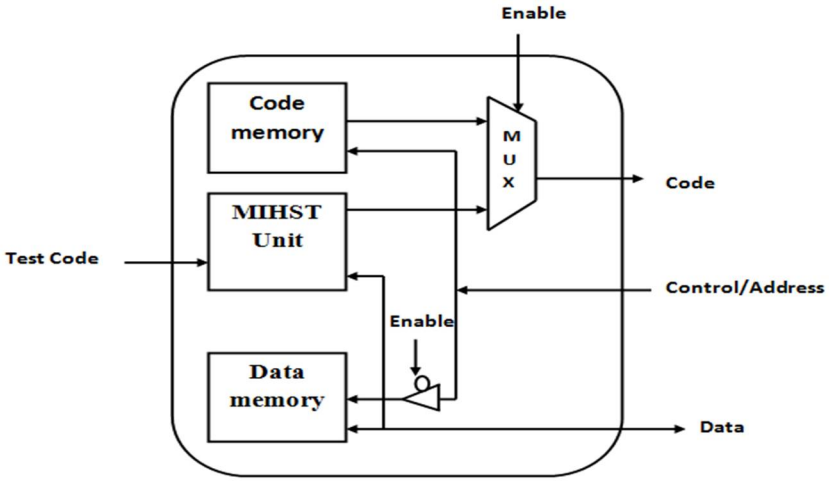

Fig-5: MIHST Architecture

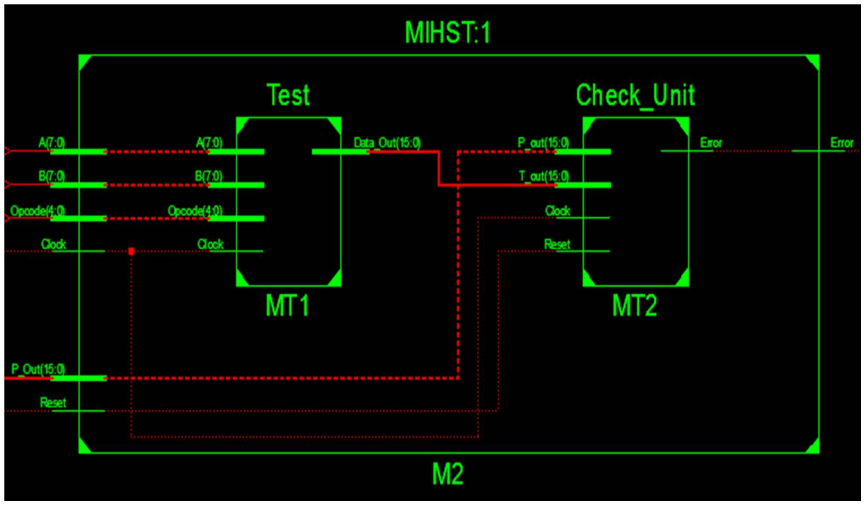

Fig-6: MIHST RTL schematic

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IV. SIMULATION RESULTS

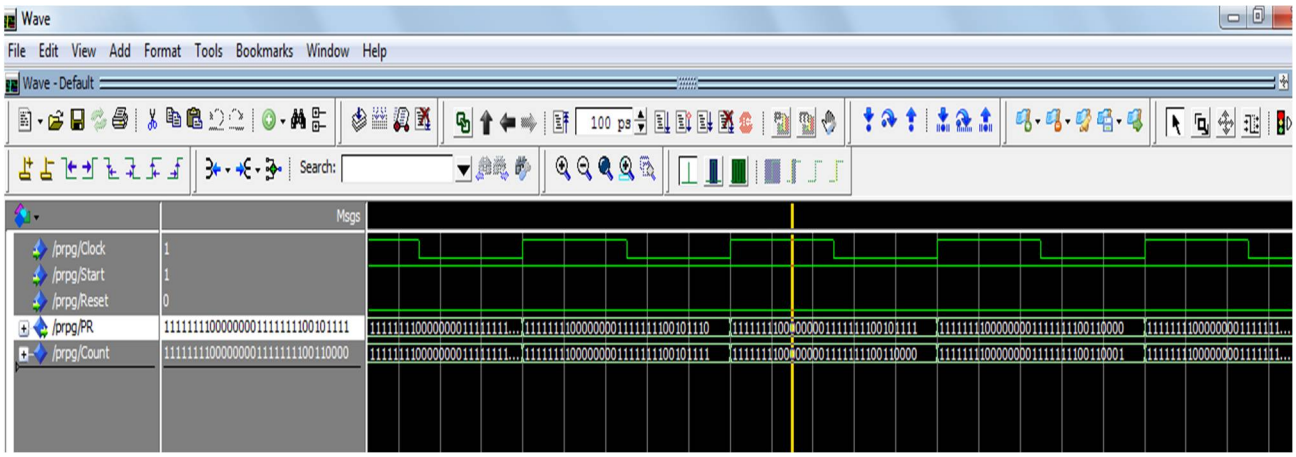

Fig-7: PRESTO simulation results

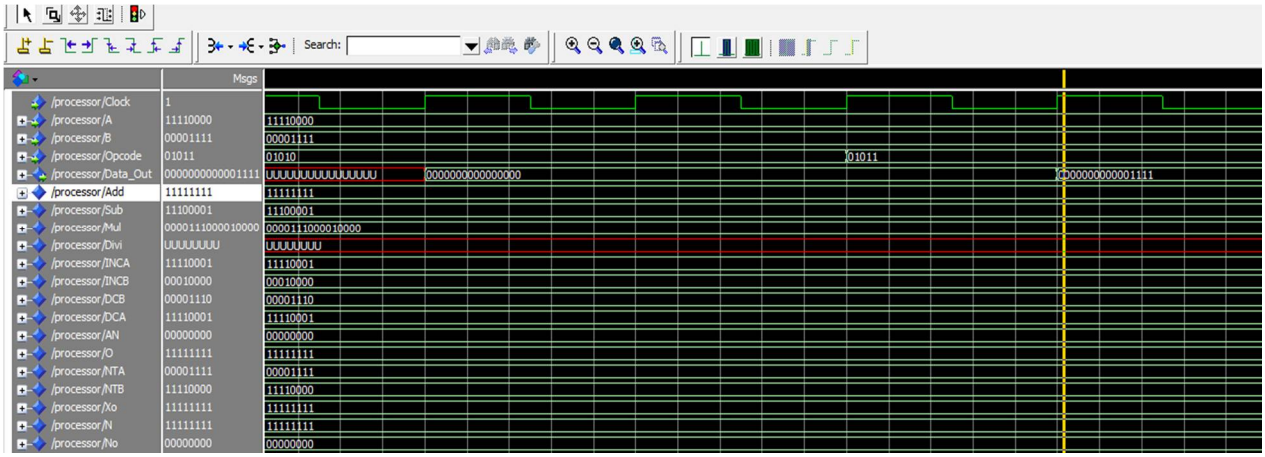

Fig-8: Test design block simulation result

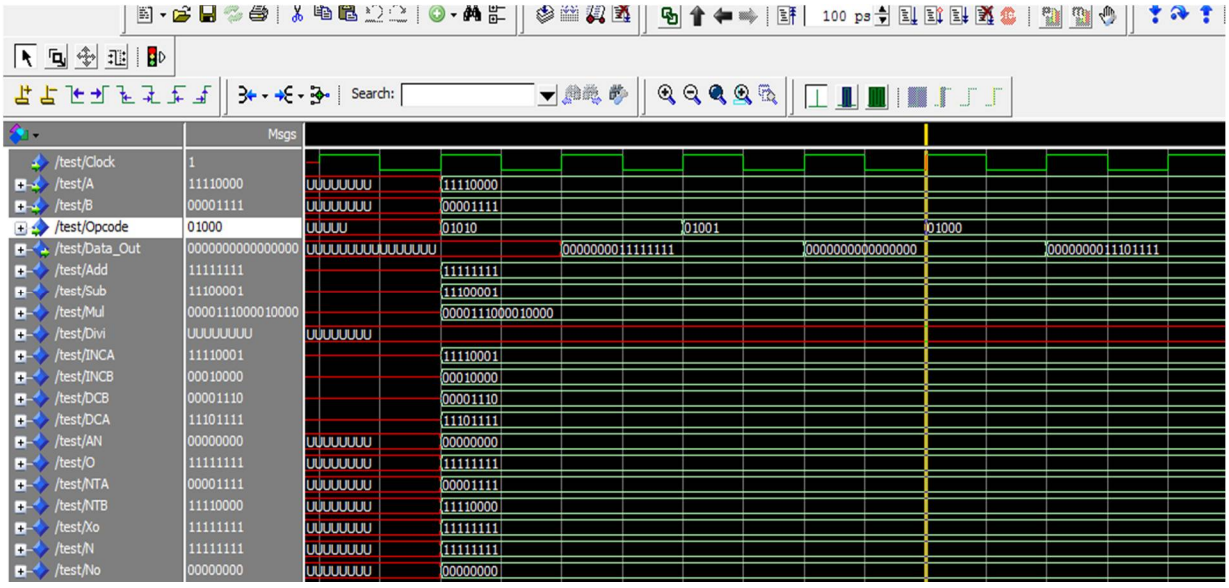

Fig-9: MIHST unit simulation result

V. CONCLUSIONS

Proposed a Test pattern generation method, where patterns are generated using PRPG. The PRESTO configuration is proposed here, it generates pattern with preselected toggling rate, i.e. the pattern produced have user distinct toggling rate. So the switching activity of sequence will be reduced due preselected toggling and power utilization is reduced. PRESTO is low power pattern generator. The MIHST architecture is developed for self test, used to test IP core of processor in SoC. MIHST approach overcomes limitations of SBST. Test cost and time is reduced using MIHST method.

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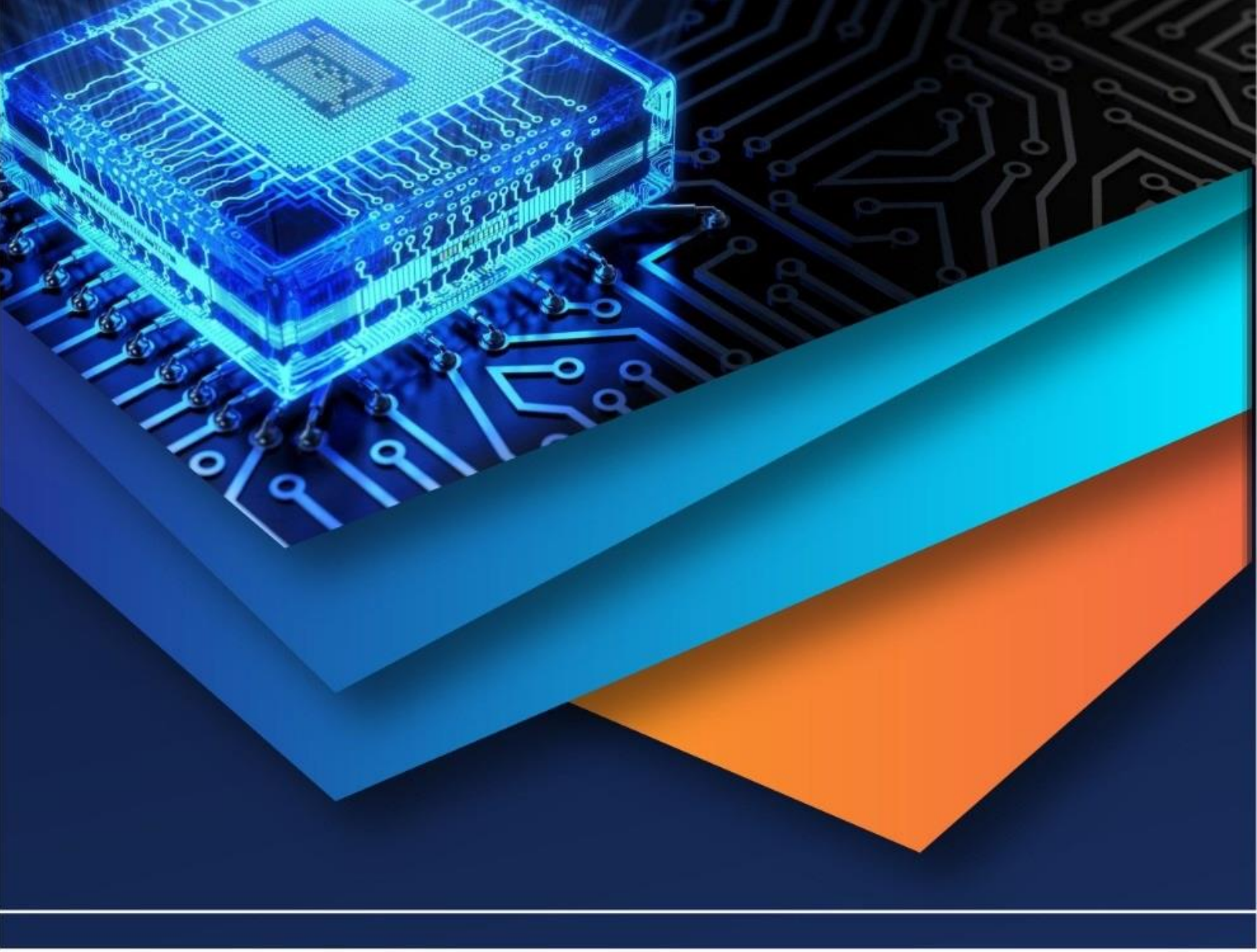

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