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Highly efficient PA and CMSA Integration for Millimeter Based networks

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Abstract*—In this work, the simulation analysis of power amplifier and circular shaped patch antenna for millimeter based networks is proposed. A beauty thought of new design of CMOS power amplifier and circular shape micro-strip antenna may largely improve the transmitter integration system and effective cost of the chip. In this paper, a three different module are proposed and analyzed through Agilent ADS tool. Firstly, power amplifier using micro-strip line as an input-output matching network is analyzed and achieves more than 25dB gain with PAE of 73%. Secondly, a circular shape patch antenna design achieves more than 10dB gain. Finally, a Co-design of PA with micro-strip antenna at 31 GHz is to relax the 50Ω impedance matching constraints and to provide S_{11} of -26dB and VSWR is 1.5.

Keywords*— Circular patch antenna; millimeter wave (MMW); CMOS power amplifier (PA)

INTRODUCTION

Recently, fastest growth of CMOS devices in microwave based industries is establishing a big new market opportunity. Good researchers are founding continuously new solutions which would be implemented into the existing wireless system networks to provide the wider bandwidth, the high quality and new added services. A millimeter wave (MMW) frequency band is the most promising technology for providing broadband wireless communications [1]. The extensive progress of CMOS technology has enabled its application in microwave and millimeter wave technologies. Presently, the CMOS technology has became one of the most attractive choices in implementing transceiver due to its low cost and high level of integration [2]. Despite of the advantages of CMOS technology, the design of CMOS transceiver in millimeter wave applications exhibits several challenges and difficulties that the designers must overcome. In addition, Kinetic performances of active devices with patch antenna have been improved, where MMW designs can be considered [3].

Power amplifier (PA) is an important unit of the wireless transceiver, so designing a high performance PA is the key to improve performance of wireless receivers [4]. However, the designing and implementation of CMOS PA is very difficult. Demands in different aspects of the PA require designers to consider comprehensively how indicators can compromise between one another. Today, several authors are designing a power amplifier using LC matching networks and to achieve maximum PAE of 50%. In [5], two stage class AB PA is designed for 3G applications and achieves PAE of 50%. In this work, Class AB PA is selected as it displays higher power efficiency as well as linearity. Single-ended two-stage amplification form is used in this design. In order to achieve more efficient match, micro-strip line is adopted. This design has demonstrated a simple structure, but with high stability, as well as superior overall performance, which can be used as a transmitter for millimeter and microwave applications.

ANALYSIS OF POWER AMPLIFIER

Power amplifiers involve a balancing of many different parameters, including power added efficiency (PAE), maximum output power, linearity, maximum stable gain, power dissipation, stability, input/output matching, and breakdown voltage. As with many RF component designs, these requirements are often in conflict with one another. As the fulfill these requirements of PA design, different topologies like common source (CS), Common Gate (CG) etc. are available which are briefly discuss below.

Class-AB Topology

The common source (CS) and common gate (CG) topologies are two popular architecture choices which are widely used for

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PA design. Common source structure is used in this circuit. Meanwhile, in order to achieve the gain of more than 20 dB, power amplifier use single-ended two-stage amplification form. Single-ended topology can be avoided application of the balanced-unbalanced transformer [6], which could simplify the integration process and improve the cost efficiency per unit of PA. For matching using LC networks as input and output achieves PAE up to 50% but if implement 50Ω transmission line like micro-strip, CPW etc then it is possible to achieve PAE of 80%. In a Micro-strip line, conductor losses increase with increasing characteristic impedance due to the greater resistance of narrow strips. Conductor losses follow a trend that is opposite to radiation loss with respect to W/h. The power handling capacity of a micro-strip is limited by heating caused because of ohmic and dielectric losses and by dielectric breakdown. An increase in temperature due to conductor and dielectric losses limits the average Power of the Micro-strip line, while the breakdown between the strip conductor and ground plane limits the peak Power. In order to determine the optimum load, the transistor should have its input matched to the source using a micro-strip line at the centre frequency of the operating band is connected to a variable load resistance at the output node.

CIRCUIT DESIGN

A 31GHz two stage of CMOS PA is designed using 90nm commercial TSMC design kit in Agilent advanced design system. Fig.1 shows the overall PA circuit, it includes bias circuit, input matching network, and output matching network

and inter-stage matching network. A two-stage amplifier bias circuit is composed of MTL1, MTL2, MTL6 and DC power VGG1, VGG0. The gate values of VGG1 and VGG2 are chosen as 0.6V. A suitable quiescent point is provided, so the amplifier works at the mode of Class AB. By improving the input matching, it is possible to achieve the maximum power efficiency, diminish signal distortions caused by reflection, and hence enhance linearity, further stabilize the circuit. T-circuit network is composed of C1, C2and MTL1, which could

be achieved by using input impedance and source impedance (50Ω) match and achieves the good reverse isolation (S_{11}) is -34dB and 50Ω input impedance with the help of equation given below and its simulation results are shown in Fig.2 and Fig.3 respectively.

$$Zin = \frac{1}{g_m + jwC_{gs}} \quad (1)$$

$$S_{11} = 20.log_{10}\left(\left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right|\right) \quad (2)$$

The high pass L-type output matching network is composed of C4and MTL6, so load impedance of 50 Ω is transformed to the best load value, thus the required output power can be obtained. Selecting on-chip inductor is the key to design a matching network, because it determines the quality of the matching network. The inter-stage L-type matching network is composed by MTL4 of the first stage amplifying circuit and MIM (Metal-Insulator-Metal) capacitor C3 [7]. The best power transmission is achieved by inter-stage matching between the first stage and the second stage. This matching network could also be used to adjust the amplifier gain flatness [8]. The maximum of S_{21} is reached nearby the centre frequency of 31GHz by adjusting capacitance, thus the best power added efficiency of 73% can be achieved that is shown in fig4 and fig5 respectively. Parasitic capacitances of input and output RF bond pads are also considered in the circuit simulation. In this simulation, we have chosen design specifications and technologies under low supply voltage of 1V are shown in Table1. All parametric values of micro-strip lines from MTL1 to MTL6 are shown in table2.

Table1 Shows specifications and technology of MOS transistors

	Device Width (µm)	**Length (µm)**	**Biasing (V)**
M1	36	.09	1
M2	21	.09	1

Table2 shows parametric values of micro-strip lines

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Micro-strip line	W (mm)	L(mm)
MTL1	0.86	4
MTL2	0.62	2.5
MTL3	0.62	2.5
MTL4	0.62	2.5
MTL5	0.62	2.5
MTL6	0.62	2.5

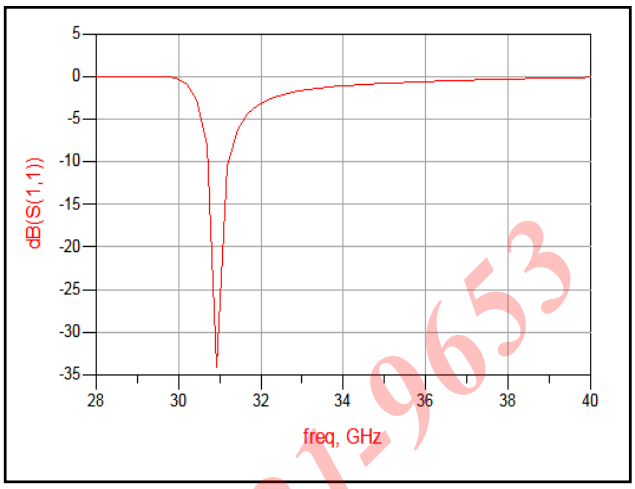

Fig.2 Return loss Vs frequency at 31GHz of PA

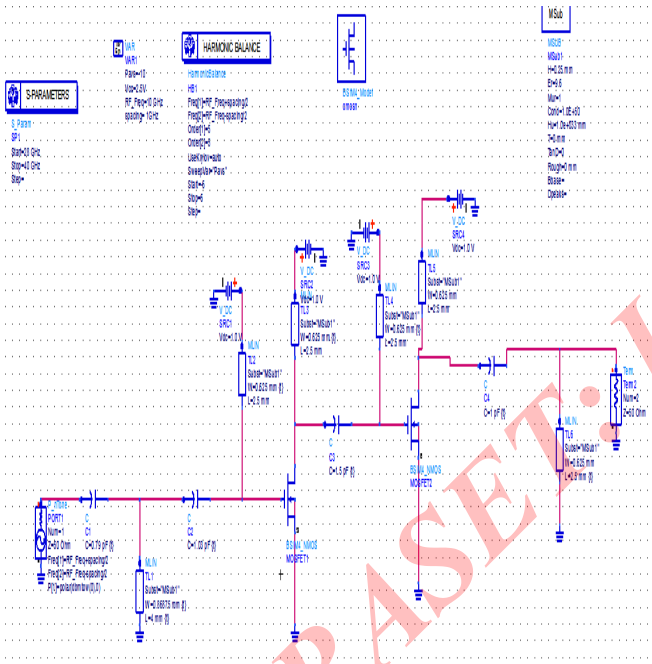

Fig.1 Schematic circuit of PA at 31GHz

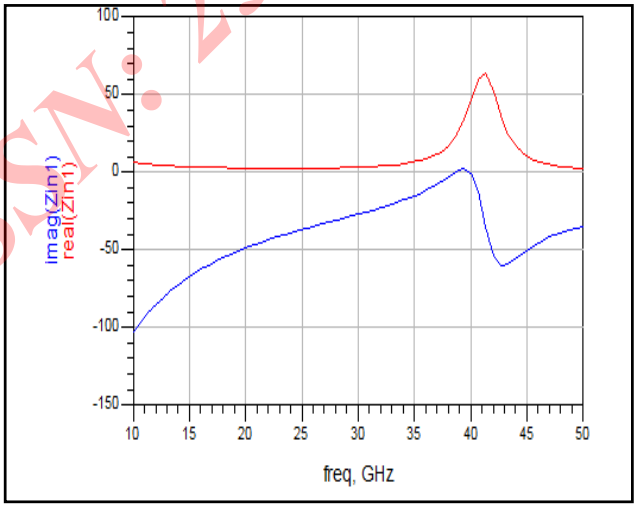

Fig.3 Input impedance variation with frequency of PA

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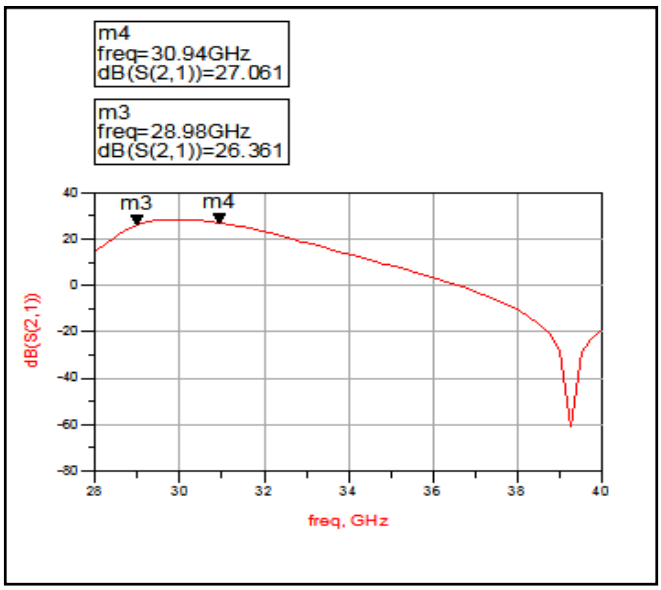

Fig.4 Forward gain Vs frequency of PA

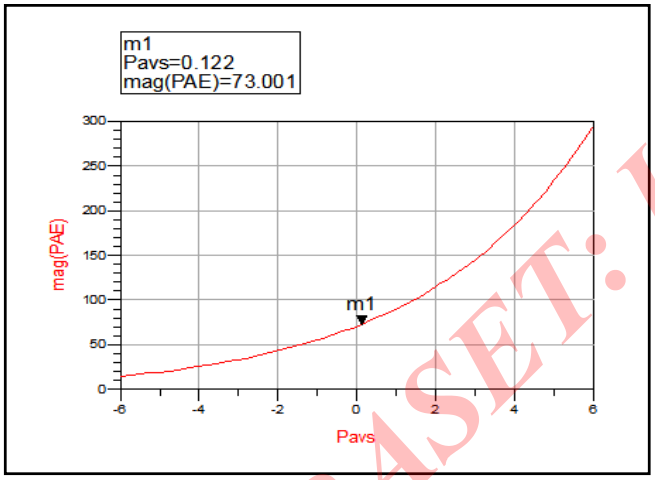

Fig.5 PAE Vs Pin (dBm)

DESIGN CONSIDERATION OF THE ANTENNA

The micro-strip antenna is a small electrically antenna that has a number of advantages over the other antennas i.e. lightweight, inexpensive, and easy to integrate with active devices to improve the system reliability [9]. In this paper, we have design a circular patch antenna at 31GHz with new type of feeding and simulated in ADS tool. All the design work taken a RT durroid substrate with thickness of t = 0.245 mm at the height h = 10mil above a lossless ground conducting layer. The dielectric between metal layers is assumed to have ϵ_r = 2.36 and tanδ = .002. At 31GHz, a 50Ω feed line given these parameters would have a width and length is 2mm and 0.7mm respectively and the final dimensions of the patch are a length L = 2.2mm and a width W = 2.4mm respectively. The 3D view of patch antenna is shown in Fig.6. The resulting return loss (S_{11}) -38.08dB and gain of more than 10 dB are shown in fig7 and fig8 respectively. The surface current distribution shows direction of radiation of the antenna and it can be seen in fig9.

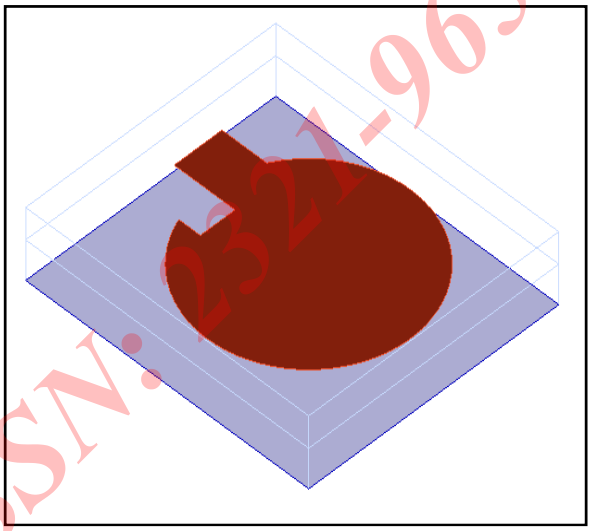

Fig.6 3D view of the designed patch antenna at 40GHz

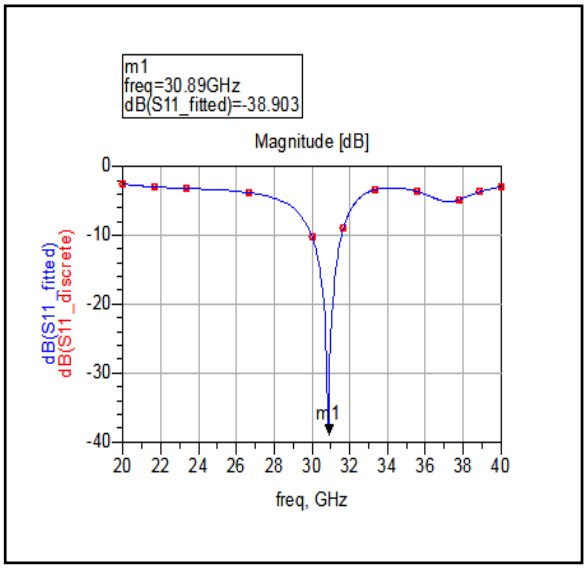

Fig.7 Return loss Vs frequency

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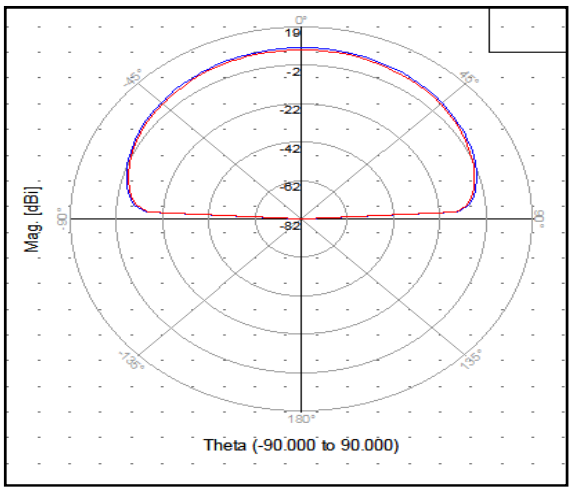

Fig.8 Radiation pattern of antenna at 31GHz

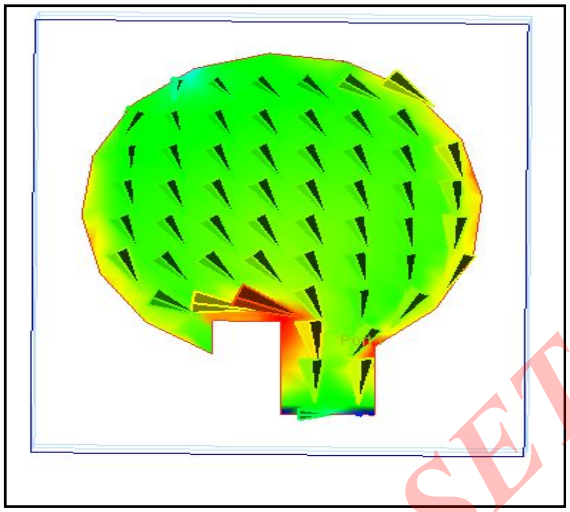

Fig9. Surface current distribution at 31GHz

PROPOSED STRUCTURE OF THE COMMUNICATION LINK

According to previously discussed the analysis of PA and circular patch antenna, integrated the design as the single structure and check the performance of complete design with the support of simulation tool in ADS2012. It is well known that if we design a transmitter system then 50Ω matching is essential for passes the signal from power amplifier to the antenna via transmission line. So it reveals from the simulation results of complete design, we have achieved real and imaginary impedance with return loss (S_{11}) of -25dB by proper impedance matching of 50Ω constraints. The complete schematic design for transmitter system at 31GHz is shown in Fig.10. All simulation results of transmitter system are also given below in Fig.11 and Fig.12 respectively.

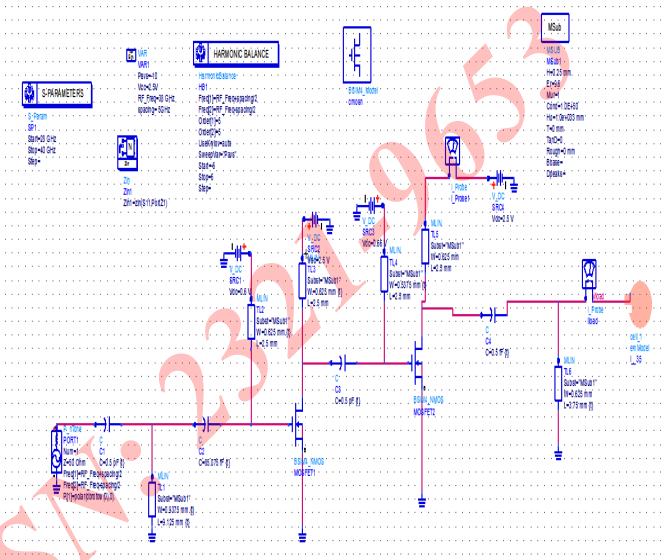

Fig.10 Complete design of receiver system at 40GHz

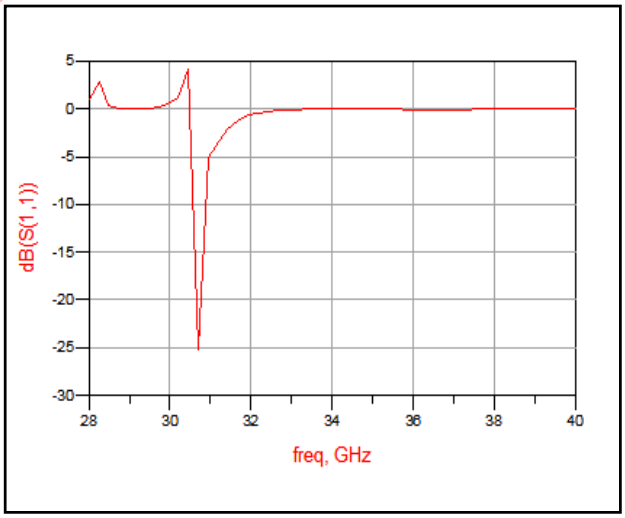

Fig.11 Return loss Vs frequency

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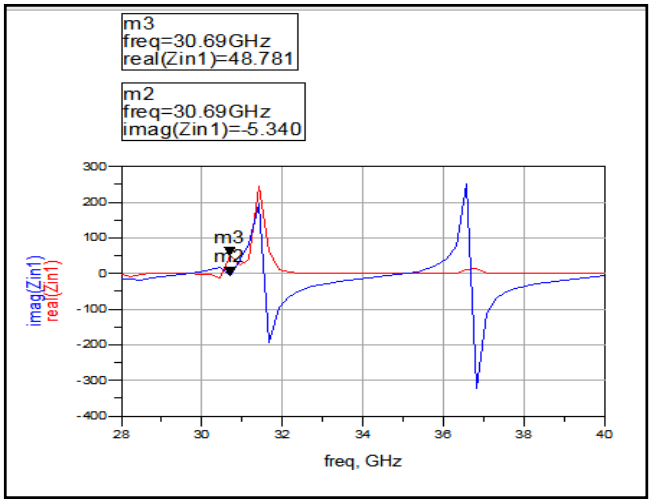

Fig.12 Impedance Vs Frequency

CONCLUSION

The complete transmitter system is designed for MMW applications in this paper, based on CMOS technology. The single-ended two stages of PA are designed using 90nm CMOS process at 31GHz in this circuit. Performance standards are met for this new design technique. Simulation results of the designed circuit are shown that gain of 27dB, S_{11} of –33dB and PAE of 73% with the DC power dissipation of 25mW under 1V power supply. The proposed method of receiver system in MMW applications, increases the level of system integration, reduces chip area and increases the overall efficiency.

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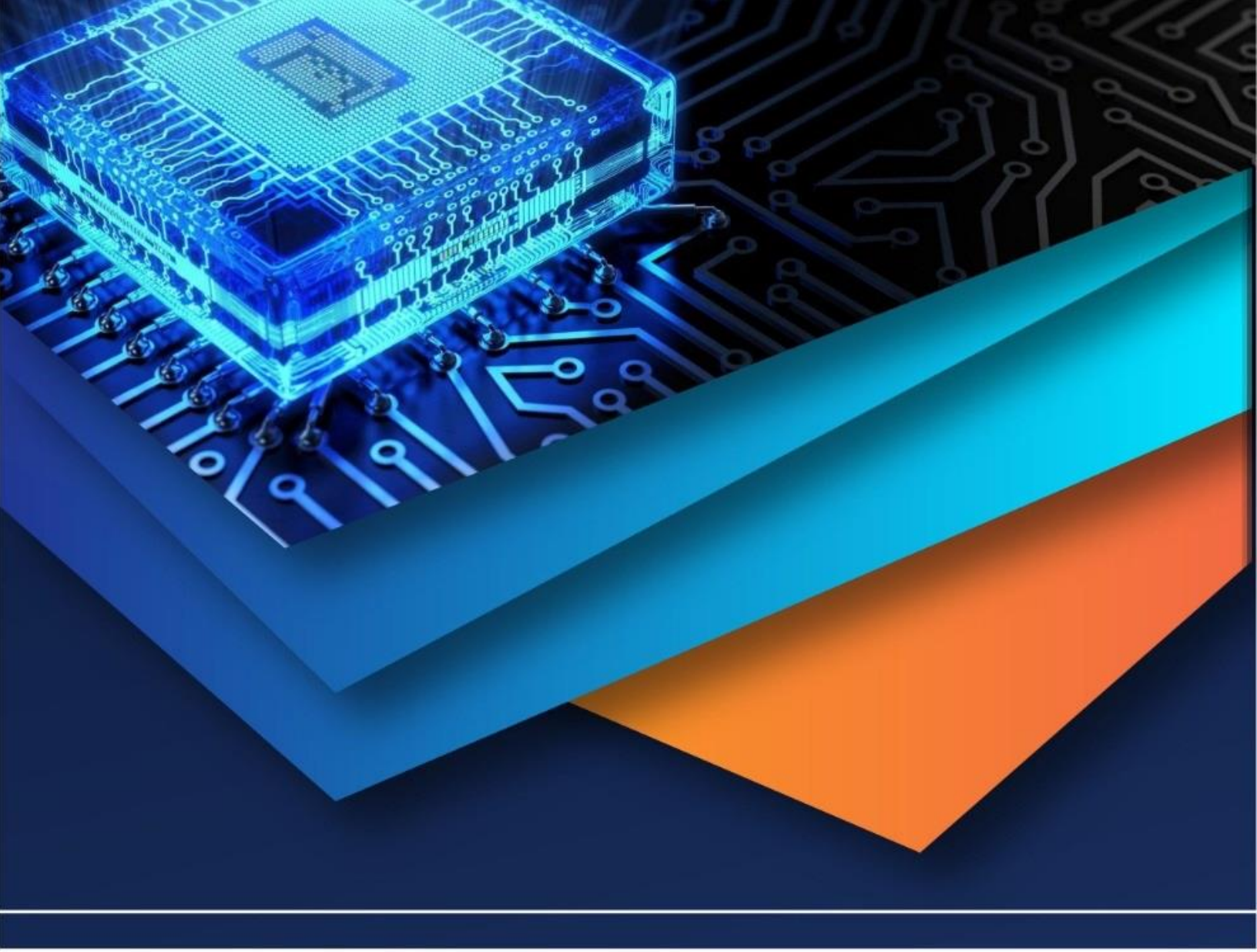

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