iJRASET
International Journal For Research in Applied Science and Engineering Technology

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

**Volume:** 4 **Issue:** VIII **Month of publication:** August 2016

**DOI:**

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

# Design and Analysis of a two stage Wideband LNA in 130-nm CMOS Technology

Jagdish Rokde[1], Prof. Sanjay Tembhurne[1]
[1]Student, M-Tech 4th Sem,G. H. Raisoni Academy of Engineering and Technology Nagpur, Maharashtra, India

***Abstract*— This paper presents a Two stage wideband low-noise amplifier (LNA). Wideband input-impedance matching was achieved using lumped component. Cascode Topology(CS transistor cascade with CG transistor) is used. Inductive degeneration techniques for second stage of WLNA. RLC matching technique used for input, output and inter-stage matching. Active bias or transistor biasing technique used for biasing of transistor. Supply voltage used is 1.8V. Wideband frequency range is 1.6-10.6GHz.Theoretical analysis shows that the frequency response of the power gain, as well as the noise Fig. (NF), can be described by second-order functions with quality factors or damping ratios as parameters, Implemented in 130 nm CMOS Technology. This achieves S11 below-10 dB, S22 below -10 dB, flat S21 of above 30dB, and flat NF of 3.3dB over the 3.1–10.6GHz band. The analytical, simulated, and measured results are mutually consistent.***

***Keywords*—CMOS, feedback, flatness, low-noise amplifier (LNA), matching, noise Fig.(NF), series peaking, wideband.***

## I. INTRODUCTION

Recently, wideband technology has attracted much attention because of its high data-rate transmission capability. In such a wideband system, a low-noise amplifier (LNA) with wideband input-impedance matching is a must. The need to reduce the size, cost and power consumption of portable electronics is the driving force behind the motivation to integrate RF front-end and digital signal processing on a one chip. CMOS technology is the most attractive solution due to the low cost, high density and high performance in terms of speed. Typically, high gain and low noise in LNAs involves high power dissipation, which is not desirable in portable electronics. At high frequencies, CMOS LNAs typically have signal loss through the drain/source to substrate parasitic which degrades the NF and power gain.

In some applications broadband is not required, therefore to reach this goal, various wideband-matching techniques for wideband LNAs have been proposed. For example, a cascade CMOS LNA with a band pass response at the input for wideband impedance-matching has been reported. Such topology incorporates the input impedance of the cascode amplifier as a part of the filter. However, the adoption of the filter at the input requires a number of reactive elements, increasing die-size and the noise Fig. (NF) due to the finite quality (Q) factor of the passive components when implemented on-chip.

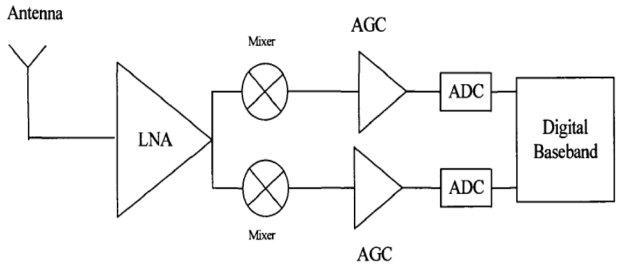



Fig.1. Block diagram of receiver

In the receiver section the mixture is present after the LNA (Low Noise Amplifier). The objective behind the mixture is to remove the carrier from the signal. Then there is an Automatic Gain Control block and the main purpose behind this is to balance the amplification or attenuation of received signal. The purpose of ADC is to covert the analog signal into the digital data which is then fed to DSP section to process the transmitted data.LNA is placed at front end which reduce then losses in the feed line. At the receiver the input signal is 1st amplified by LNA then process through the further stages of receiver. As much as ideal is the LNA is designed, more ideally the signal is covered at the receiver. The Low Noise Amplifier is the chief component of the receiver section which must give high gain, low noise figure, stability with linearity also low power consumption.

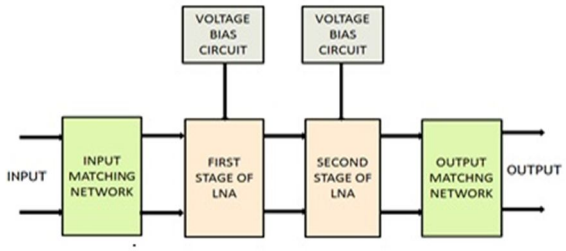



Fig.2. Block diagram of LNA

The performance of RF receiver is depend on the hoe effectively the Low Noise Amplifier is performing. In the RF receiver, the noise effect from the various subsequent stages of the receiver is reduced by Low Noise Amplifier. Therefor it is very necessary for LNA to boost the desired signal and remove the distortion, so that the signal can be retrieved in the later stages.

## II. OVERVIEW

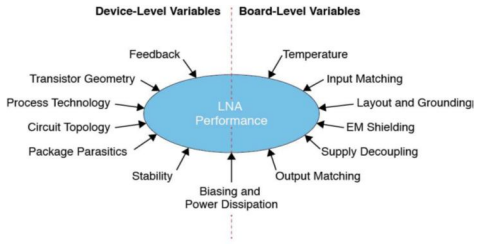



Fig.3. LNA Performance Variable

Fig.3 shows the set of variables that affect LNA performance. It is up to the designer to impact of environmental variables, while finding the most appropriate trade−off between competing characteristics to optimize receiver sensitivity and selectivity, and maintaining information integrity. Low noise amplifiers (LNAs) play a key role in radio receiver performance. The success of a receiver's design is measured in multiple dimensions: receiver sensitivity, selectivity, and proclivity to reception errors. The RF design engineer works to optimize receiver front−end performance with a special focus on the first active device. To illustrate the practical challenges, performance trade−offs for three popular LNA topologies and two process technology implementations are examined. Five characteristics of LNA design are under the designer's control and directly affect receiver sensitivity: noise Fig. , gain, bandwidth, linearity, and dynamic range. Controlling these characteristics, however, requires an understanding of the active device, impedance matching, and details of fabrication and assembly to create an amplifier that achieves optimal performance with the fewest trade−offs.

## III.LNA TOPOLOGIES

Common−source, common−gate, and cascode are three prevailing LNA topologies. Table 2 provides a concise comparison based on the most relevant considerations for LNA design.

TABLE I.
COMPARISON THREE LNA TOPOLOGIES

| Characteristic | Common-Source | Common-Gate | Cascode |
|---|---|---|---|
| Noise Figure | Lowest | Rises rapidly with frequency | Slightly higher than CS |
| Gain | Moderate | Lowest | Highest |
| Linearity | Moderate | High | Potentially Highest |
| Bandwidth | Narrow | Fairly broad | Broad |
| Stability | Often requires compensation | Higher | Higher |
| Reverse Isolation | Low | High | High |
| Sensitivity to Process Variation, Temperature, Power Supply, Component Tolerance | Greater | Lesser | Lesser |

The cascode amplifier is the most versatile of the three topologies. It provides the most stable signal gain over the widest bandwidth with only a slight sacrifice in noise Fig. performance and design complexity. The common−source transistor is sized to deliver the best possible noise Fig. , but that advantage often comes at the cost of greater sensitivity to bias, temperature, and component tolerances. The raw transistor rarely has its Yopt coincide with Yin. To minimize the need for external noise matching circuit components, the LNA designer manipulates transistor construction (gate finger multiples, finger dimension, interconnects, and layout), RF feedback, and package parasitics to have Yopt simultaneously converge on Yin and the system's characteristic admittance.

Careful insertion of source degeneration feedback also improves amplifier stability and linearity at the expense of gain, especially at higher frequencies. Too much or too little feedback, however, degrades stability and performance; therefore, the LNA designer seeks the optimal value. This design feature allows the user to find a much better trade−off between amplifier noise Fig. , gain, and input return loss.

The cascode amplifier combines the common−source stage previously described with a common−gate transistor designed for optimal linearity. The cascode amplifier, however, becomes greater than the sum of its parts when the common−source transistor is also designed to pre−distort the common−gate transistors. These design features greatly ease LNA implementation and improve stability, bandwidth, and linearity.

## IV. BIAS BIASING NETWORK DESIGN

Setting the LNA bias is the first most critical step in implementation. Most LNA MMICs have an integrated active−bias circuit that regulates bias currents over variations in supply voltage, temperature, and FET threshold voltage. Careful selection of a bias point, however, is still required to find the best compromise between gain, NF, and linearity for any given application. There are several important considerations when approaching the task of input matching. Noise Fig. degradation can be mitigated by limiting the number of elements between the antenna and LNA input. A high−Q input matching network provides an optimal noise Fig. and gain performance because of the minimal loss, but these networks are often quite sensitive to variations in process, voltage, temperature, and component value.

## V. INPUT AND OUTPUT MATCHING

Careful design produces a device with well−controlled input and output impedances at which the optima of various important performance characteristics come close to coinciding. There are several important considerations when approaching the task of input matching. Noise Fig. degradation can be mitigated by limiting the number of elements between the antenna and LNA input. A high−Q input matching network provides an optimal noise Fig. and gain performance because of the minimal loss, but these networks are often quite sensitive to variations in process, voltage, temperature, and component value. There are a number of performance parameters that show to what extent the impedances are matched. Firstly, the Reflection Coefficient which by definition is the ratio of the reflected wave to the incident wave (Equation 1.), but can also be expressed in terms of impedances. It is a complex entity that describes not only the magnitude of the reflection, but also the phase shift.

$$\Gamma_L = \frac{\text{Reflected wave}}{\text{Incident wave}} = \frac{Z_L - Z_S}{Z_L + Z_S} \quad (1)$$

This is the load reflection coefficient with respect to the source impedance. It is also commonly expressed with respect to the characteristic impedance (Z0). When the load is short-circuited, maximum negative reflection occurs and the reflection coefficient assumes minus unity. In contrast, when the load is open-circuited, maximum positive reflection occurs and the reflection coefficient assumes plus unity. In the ideal case, when ZL is perfectly matched to ZS, there is no reflection and the reflection coefficient is consequently zero. A closely related parameter is the Voltage Standing Wave Ratio (VSWR). The VSWR is defined as the ratio of the maximum voltage to the adjacent minimum voltage of that standing wave (Equation 2). Knowing the domain of the reflection coefficient, it follows that when there is no reflection as in a perfectly matched system; VSWR assumes its minimum and ideal value of 1.

$$VSWR = \frac{|V|_{max}}{|V|_{min}} = \frac{1 + |\Gamma_L|}{1 - |\Gamma_L|} \quad (2)$$

The source- and load impedances are fixed; the objective is to design the input matching network so that ZS matches Z1 and the output matching network so that ZL matches Z2. In other words Z1 and Z2 respectively, are transformed to perceptually match the input and output impedances of the transistor. According to the Maximum Power Theorem, the maximum power transfer will occur when the reactive components of the impedances cancel each other, that is when they are complex conjugates. This is suitably called conjugate matching.

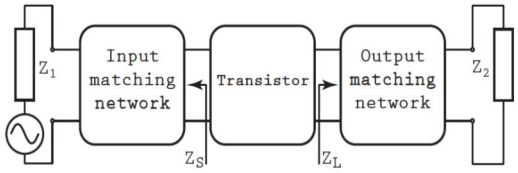



Fig.4. Matching network in microwave amplifier.

To achieve the conversion with an impedance matching network of passive components, there are primarily three options. Firstly, there is the L-match. Its advantage is the simplicity, but that is simultaneously its downside as well because it has only two degrees of freedom. Since there are only two component values to set, the L-match is restricted to determining only two out of the three associated parameters: impedance transformation ratio, center frequency and Q. To acquire a third degree of freedom, it is therefore desired to cascade another L-match stage. By doing so, another two types of impedance transformation matches are encountered: the π-match and the T-match.

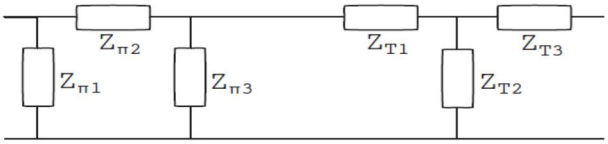



Fig.5. Cascade π match and T match network.

The advantages with the T- and π-match configurations do not end with an additional degree of freedom. But because of their topology they can absorb parasitic reactance present in source or load. Specifically the T-match will absorb parasitic inductance whereas the π-match will absorb parasitic capacitance. In addition it is also possible to achieve significantly higher Q compared to an L-match configuration. Another noteworthy impedance transformation option is band pass filtering where the port impedances are unequal.

## VI. SCATTERING PARAMETERS

Scattering Parameters or S-parameters are complex numbers that exhibit how voltage waves propagate in the radio-frequency (RF) environment. The characteristics of the 2-port is represented by a set of four S-parameters: S11, S12, S21 and S22, which correspond to input reflection coefficient, reverse gain coefficient, forward gain coefficient and output reflection coefficient respectively. S-parameters, on the other hand, are measured under matched and mismatched conditions. Under such circumstances, it becomes necessary to measure the parameters.


Fig.6. A two port with incident wave's a1 & a2 and reflected waves b1 & b2

Referring to Fig. 6, these measurements are carried out by measuring wave ratios while systematically altering the termination to cancel either forward gain or reverse gain according to the following equations:

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0} \quad (3)$$

$$S_{12} = \frac{b_1}{a_2}\Big|_{1=0} \quad (4)$$

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0} \quad (5)$$

$$S_{11} = \frac{b_2}{a_2}\Big|_{a_1=0} \quad (6)$$

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad (7)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad (8)$$

## VII. THE QUALITY FACTOR

The Quality Factor (Q) is a descriptive parameter of the rate of energy loss in complete RLC networks or simply in individual inductors or capacitors. For the latter, Q is a measurement of how lossy the component is, that is how much parasitic resistance there is. So it follows that in applications where loss is undesirable, high Q components are advantageous. The equations for calculating Q are:

$$Q_{RLC} = \omega \frac{E_{tot}}{P_{avg}} \quad (9)$$

$$BW = \frac{\omega_0}{Q_{RLC}} \quad (10)$$

$$Q_L = \frac{X_L}{R} = \frac{\omega L}{R} \quad (11)$$

$$Q_c = \frac{|X_c|}{R} = \frac{1}{\omega CR} \quad (12)$$

## VIII. CIRCUIT DESIGN

Fig.7 shows a Two-stage WLNA is employed to simultaneously achieve a high gain and a wide band. While designing Low Noise Amplifier (LNA), we needs to put different aspects into consideration, like high gain, low noise figure, better input and output matching, stability and linearity. All these factors are interdependent on each other. It is therefore it must require to set appropriate balance between these parameters. Figure below shows the schematic for Wideband LNA ,the source terminal of each NMOS transistor is grounded, the lumped components are used for designing the circuitry of LNA. While designing Low Noise Amplifier (LNA), we needs to put different aspects into consideration, like high gain, low noise figure, better input and output matching, stability and linearity. All these factors are interdependent on each other. It is therefore it must require to set appropriate balance between these parameters.

Figure below shows the schematic for Wideband LNA ,the source terminal of each NMOS transistor is grounded, the lumped components are used for designing the circuitry of LNA. Then there is pair of transistors (M1, M3). Thus M1 and M3 together forms the first stage of LNA. Also the topologies used by these transistors are common source topology. For the input impedance matching part π- matching is used as shown in the input side. Then the combination of R and C forms the RC negative feedback which provides the linearity. The first stage of LNA consists of self-biasing circuit which consists of two inductors which give the perfect short for AC current. The biasing is provided by the Active biasing with transistor (M6)

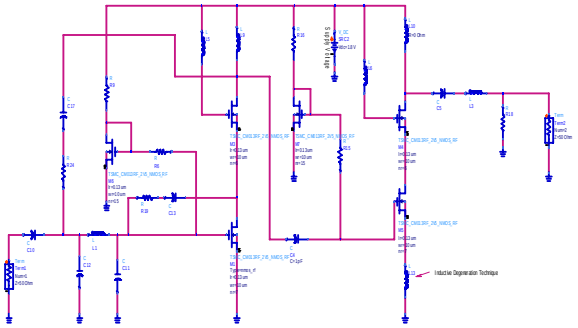


Fig.7. Designed Two Stage WLNA Schematic

This biasing provides the proper biased power supply to transistor. Then transistors (M4, M5) form the second stage of LNA which is combined with first stage by the intermediate stage. This intermediate stage forms by the capacitor. 1.8V supply is given to the circuit. Then for the output matching part the output matching is done. Which provide the proper matching. By carefully choosing the size of the transistor and with proper biasing biasing conditions, the 50Ω impedance matching can achieved. Π- matching is used to provide proper matching to transfer the power from source to load. RC- negative feedback is used for stability of circuit. Transistor/Active biasing is used for providing proper biasing .Two stages of LNA. Output matching is present at output side for matching part.

## IX. RC NEGATIVE FEEDBACK

The RC feedback LNA is shown. Uses negative feedback which gives linearity. There are two types of the feedback positive feedback and negative feedback. This design consists of negative feedback. Negative feedback gives the stability of to the circuit

because in the negative feedback the output get subtracted from the input. The feedback gives the stable gain. In the RC feedback the capacity is used to provide the proper gate voltage. Due to the negative feedback the linearity comes in the result. It gives stability. This stage require the small die area. Also this topology gives the low noise figure than other topologies

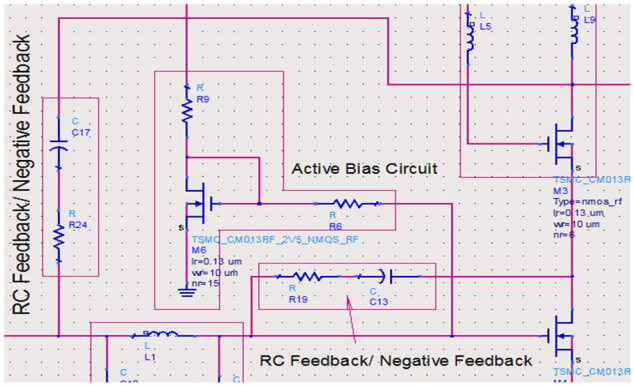



Fig.8. Input Reflection Coefficient

## X. TWO STAGE CASCADED LNA

There are number of topologies like cascade topology, cascode topology, common source topology. The designed contain one of topology cascade topology, in this topology number of stage of LNA to increase the gain factor and to balance the other parameters. Figure show the cascade topology.

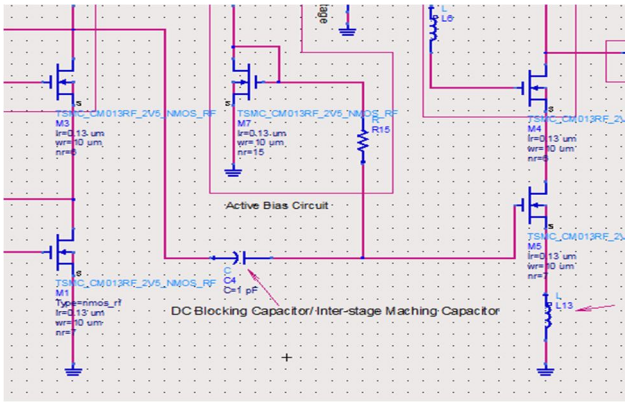



Fig.9. Two Stage Cascaded LNA

## XI. SIMULATION RESULTS AND MEASURMENT

It is simulated using Advanced Design System (ADS) 2009. The simulation recorded that the amplifier gain S21 is 31.19dB. The input return loss S11 is -10.029dB, overall noise Fig. (NF) is 3.589dBand the output return loss S22 is -19.11dB.The reflection loss S12 is - 74.450dB. These values were within the design specification and were accepted. The outputs S-parameter are shown below.

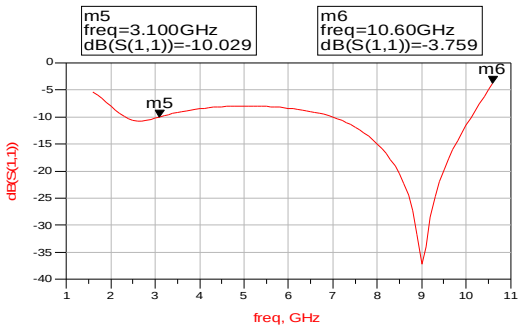



Fig.10. Input Reflection Coefficient

Volume 4 Issue VIII, August 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

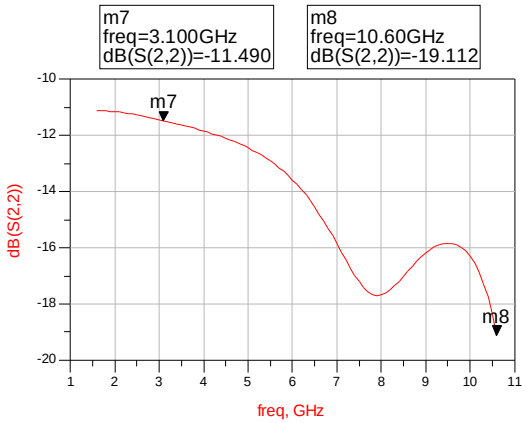



Fig. 11. Output Reflection Coefficient

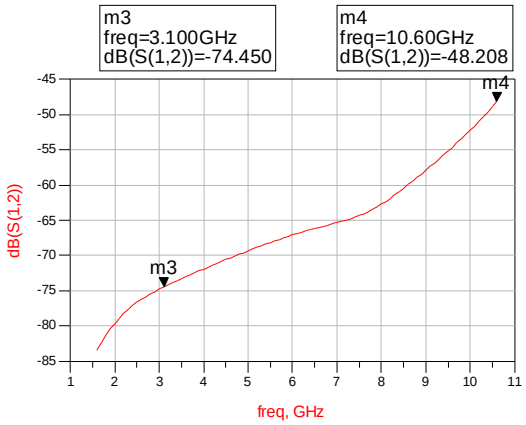



Fig.12. Reverse Isolation

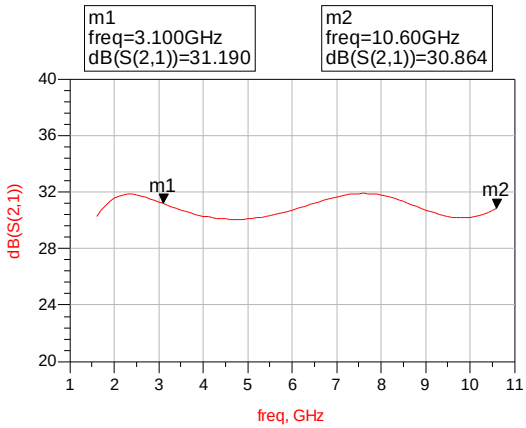



Fig.13. Power Gain

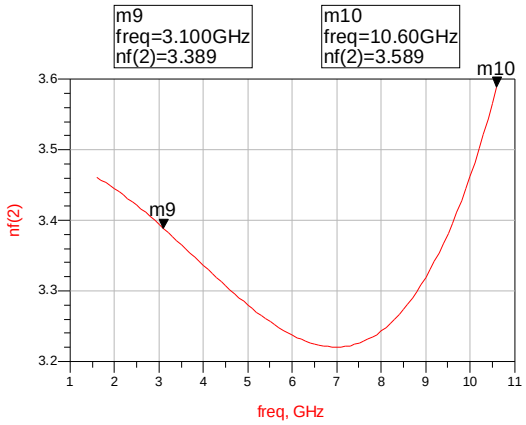



Fig.14. Noise Fig.

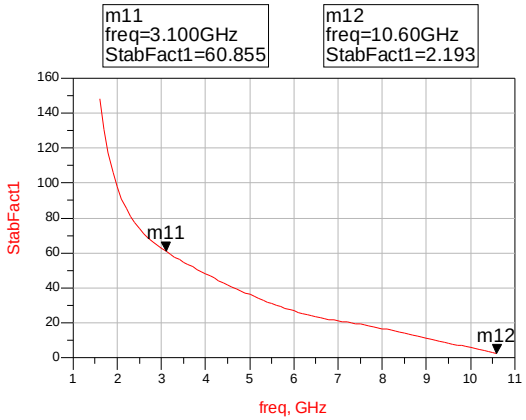



Fig.15. Stability

## XII. CONCLUSION

The 1.6-10.6GHz LNA has been developed successfully and the circuit contributed to the front end receiver at the described frequency. The two stage low noise amplifier is designed in CMOS technology. For better performance in gain of the amplifier, it is achieved by increasing the number of stages to improve the gain and noise Fig. of the design. Higher gain would expand the coverage or communication distance. WLNA designed using 130nm CMOS process. The LNA applies cascade structure with source inductive degeneration technology. Inductive degeneration techniques for second stage of WLNA. RLC matching technique used for input, output and inter-stage matching Active bias or transistor biasing technique used for biasing of transistor Supply voltage used is 1.8V. The single stage LNA is designed with 31.92 dB power gain (S21), 3.22dB noise figure (NF), -37,187dB input reflection coefficient (S11), -19.112dB output reflection coefficient (S22) and - 31.922dB reverse isolation (S21) at 3.1-10.6GHz wideband frequency.

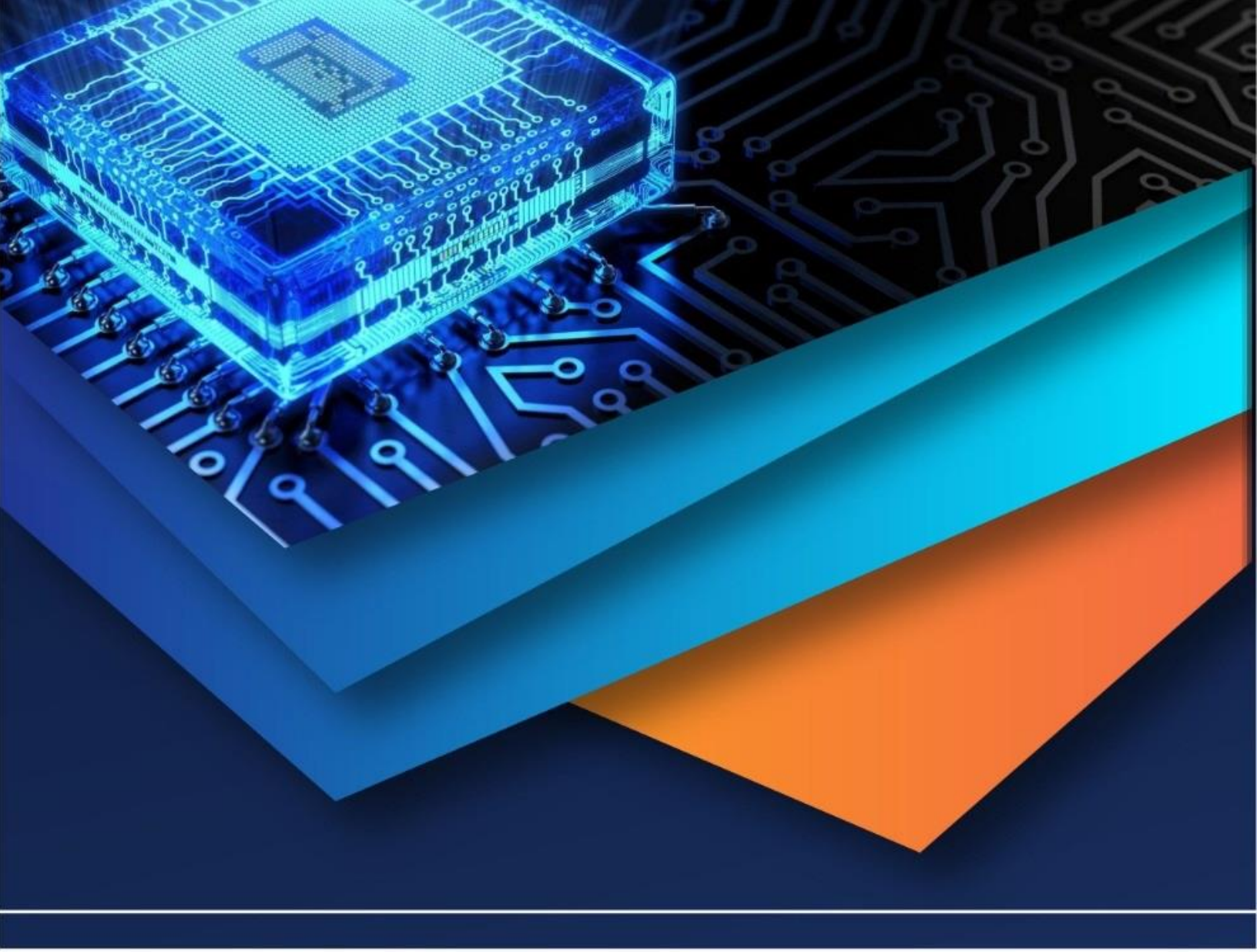
## XIII. ACKNOWLEDGMENTS

I thanks to the experts who have contributed towards development of the project.

## REFERENCES

[1] Y.-H. Yu, Y.-J. E. Chen, and D. Heo, “A 0.6-V low power UWB CMOS LNA,” IEEE Microw. Wireless Compon. Lett., vol. 17, no. 3, pp. 229–231, Mar. 2007.
[2] F. Zhang and P. R. Kinget, “Low-power programmable gain CMOS DA,” IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1333–1343, Jun. 2006.

[3] T. Chang, J. Chen, L. A. Rigge, and J. Lin, "A packaged and ESD-protected inductorless 0.1–8 GHz wideband CMOS LNA," IEEE Microw. Wireless Compon. Lett., vol. 18, no. 6, pp. 416–418, Jun. 2008.
[4] T. Chang, J. Chen, L. A. Rigge, and J. Lin, "ESD-Protected wideband CMOS LNAs using modified resistive feedback techniques with chip-on-board packaging," IEEE Trans.
[5] Y.-H. Yu, Y.-J. E. Chen, and D. Heo, "A 0.6-V low power UWB CMOS LNA," IEEE Microw. Wireless Compon. Lett., vol. 17, no. 3, pp. 229–231, Mar. 2007.
[6] F. Zhang and P. R. Kinget, "Low-power programmable gain CMOS DA," IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1333–1343, Jun. 2006.
[7] T. Chang, J. Chen, L. A. Rigge, and J. Lin, "A packaged and ESD-protected inductorless 0.1–8 GHz wideband CMOS LNA," IEEE Microw. Wireless Compon. Lett., vol. 18, no. 6, pp. 416–418, Jun. 2008.
[8] T. Chang, J. Chen, L. A. Rigge, and J. Lin, "ESD-Protected wideband CMOS LNAs using modified resistive feedback techniques with chip-on-board packaging," IEEE Trans.
[9] M. Nair, Y. Zheng, and Y. Lian, "1 V, 0.18 m-area and power efficient UWB LNA utilising active inductors," Electron. Lett., vol. 44, no. 19, pp. 1127–1129, Nov. 2008.
[10] A. Thanachayanont and A. Payne, "VHF CMOS integrated active inductor,Electron. Let., vol. 32, no. 11, pp. 999–1000, May 1996.
[11] D. DiClemente and F. Yuan, "Current-mode phase-locked loops—A new architecture," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54,no. 4, pp. 303–307, Apr. 2007.
[12] B. Razavi, Design of Analog CMOS Integrated Circuits. NewYork: McGraw-Hill, 2001.
[13] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A CMOS lownoise amplifier with reconfigurable input matching network," IEEE Trans. Microw. Theory Tech., vol. 57, no. 5, pp. 1054–1062, May 2009.
[14] T. W. Kim and B. Kim, "A 13-dB IIP3 improved low-power CMOS RF programmable gain amplifier using differential circuit transconductance linearization for various terrestrial mobile D-TV applications,"IEEE J. Solid-State Circuits, vol. 41, no. 4, pp. 945–953, Apr. 2006.
[15] D. Im, I. Nam, and K. Lee, "A CMOS active feedback balun-LNA with high IIP2 for wideband digital TV receivers," IEEE Trans. Microw. Theory Tech., vol. 58, no. 12, pp. 3566–3579, Dec. 2010.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY