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State-Space Modeling of Multi-input Converter

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Abstract-. This is a three-switch converter belongs to fifth-order family and performs boosting operation. A new two-input Boost-SEPIC DC-DC converter suitable to draw power from two different dc sources feeding a common dc-bus is presented in this paper The salient feature of the proposed converter is that both the sources are simultaneously supplying power to the downstream load at reduced ripple current. This feature is particularly attractive for dc grid application. A 48 V, 200 Watt converter performance is analyzed and compared with the simulation observations.

I. INTRODUCTION

The technological development of power electronics definitely brought back dc system in power utilization reliability, accuracy and better load regulation are main issues of modern power supply Today power electronics system are highly developed so demand of Switch-mode power converter is increasing day by day in various application such as hybrid vehicles and telecommunication power supply. In order to utilize maximum energy from more than one energy source such as fuel cell, battery, solar array and wind energy various multi input converter has been proposed in the recent year. Depending upon the applications one could select a feasible topology by considering many features like reliability, cost and flexibility. It is more advantageous to use multi-input converter rather than several independent single source converters as it results in less number of components, more stability in modern power electronics system several power sources such as battery ultracapacitor, fuel cells are used, therefore utilization of multi-input converters is inevitable. Multi input converter has advantage of higher system efficiency, high power density, light weight and small size.

The objective of this paper is to generate a two input topology by using pulsating source cell derived from six non-isolated converter such as buck, boost buck-boost, Cuk, SEPIC and Zeta. In this paper one boost pulsating source current cell (PCSC) and one SEPIC prime PWM converter are combined to transfer power from source to load [1] .The basic idea of this paper is to insert the PCSC into the energy buffer portion of the prime SEPIC converter such that both power source can transfer power to the load simultaneously. Basically any converter (except buck and boost) can be divided in to three section namely input portion IP, energy storing buffer portion EBP, and output portion OP. During one moment of switching cycle input portion will transfer power to the buffer portion and during next moment of switching cycle energy buffer portion will transfer the stored energy to the output portion without consuming any energy. This energy buffer portion may be a voltage or current buffer. There are certain rules to connect PCSC are PVSC with prime PWM converter [1].

To address some the issues various type of multi-input converter with different topology has been already reported in literature. In this paper boost PCSC and SEPIC converter based multi-input converter is proposed and then digital controller have been design to ensure load bus voltage regulation together with distribution of power by appropriate control of input dc power sources. The proposed converter has a unique feature of boosting action which is important from dc grid application point of view. Several controller design approaches have been reported in literature .However depending upon the interaction between the control loops control structure has to be chosen. If the interaction is very small then decentralized control technique will be a feasible option.

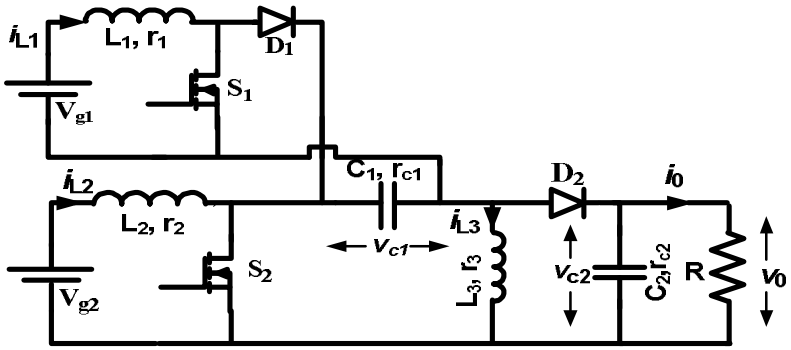

Fig. 1. Two-input dc-dc converter circuit diagram.

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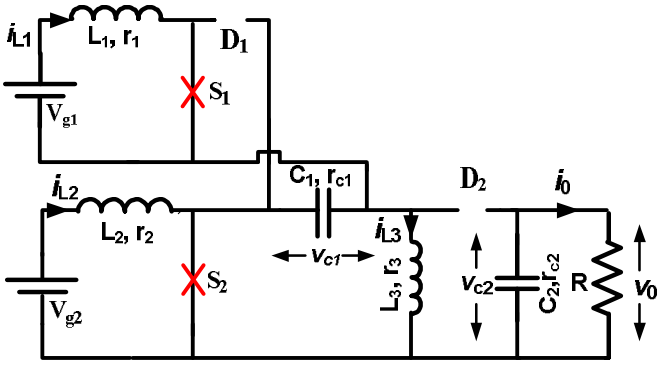

Fig. 2 Mode 1

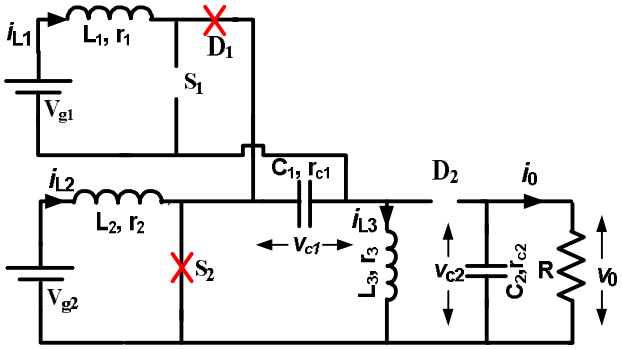

Fig. 3. Mode 2

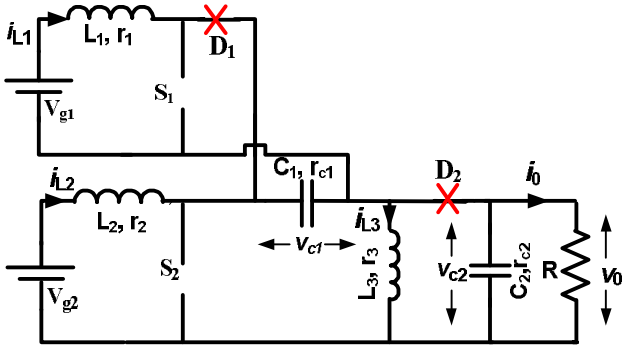

Fig. 4. Mode 3

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II. MODELING OF TWO-INPUT DC-DC CONVERTER

The proposed two-input dc-dc converter, shown in Fig. 1, has two different power sources and two switching devices with five energy storage elements and hence it forms a fifth order system. The proposed two input Boost SEPIC converter can perform bucking as well as boosting operation with respect to both the sources. The proposed converter can work in both continuous and discontinuous inductor current mode but in view of higher load power requirement this converter is analyzed for continuous inductor current mode of operation. Different modes of operation depend upon the magnitude of duty ratios. Depending upon the duty ratio three different schemes are possible. Scheme 1:$d_1>d_2$ Scheme 2: $d_1<d_2$ and Scheme 3: $d_1=d_2$. In first scheme $(d_1>d_2)$ The circuit is going to operate under four different modes in one switching cycle .In this paper scheme 2$(d_1<d_2)$ is considered in which circuit exhibits three mode operation and for scheme 3 $(d_1=d_2)$ only two modes are possible in a switching cycle.

For scheme 2 $(d_2>d_1)$ assuming switches and diodes are ideal then converter exhibits three mode of operation in a switching cycle .(a) mode-1:S_1,S_2 both are ON and diode D_1,D_2 are OFF.(b) mode-2:S_2,D_1 are ON and S_1,D_2 are OFF.(c) mode-3:S_1,S_2 both are OFF and D_1,D_2 both are ON. During mode-1 inductor L_1 and L_2 are linearly charging by their respective source voltages V_{g1} and V_{g2} and capacitor C_1 charges inductor L_3 during this mode load voltage is obtained from capacitor C_2. In mode-2 inductor L_2 charges linearly

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but inductor L_1 current will decrease linearly. During this mode of operation energy stored in inductor L_1 will transferred to buffer capacitor C_1 .Buffer capacitor will play a very important role in power processing. Depending upon the magnitude of voltage across buffer capacitor direction of power flow will be decided. In mode-3 both switches are in OFF state so both sources will transfer power to the load simultaneously.

Depending on the load demand and available power with each dc source three different cases will arise, which are: (i) $d_1 > d_2$, (ii) $d_1 < d_2$, (iii) $d_1 = d_2$. State space modeling of the converter is required to obtain mathematical model of the physical converter system. For the design of digital control system discrete time modeling is required. In this paper the $d_1 < d_2$ case is analyzed for the trailing-edge off time synchronized switching signals. If the system is linear and time invariant then for each mode of operation the power stage dynamics can easily be described by a set of state equations in matrix form given by:

$$\dot{x} = A_K x + B_K u$$
$$y = C_k x + F_k u \qquad (1)$$

where $[x] = [i_{L1} \quad i_{L2} \quad i_{L3} \quad v_{c1} \quad v_{c2}]^T$, $[u] = [V_{g1} \quad V_{g2}]^T$ and k=1,2,3 for mode-1, mode-2 and 3, respectively.

Applying volt-sec balance to all the inductors mode by mode in a switching cycle gives the voltage across all three inductor and solving equation voltage conversion ratio of this converter can be derived given by equation .2. $V_o = \frac{V_{g2}}{(1-d_2)} - \frac{V_{g1}}{(1-d_1)}$

(2)

From equation 2. it is clear that the load voltage is dependent on the both input dc sources as well as both switch duty ratio and converter is going to perform boosting operation with respect to both the power source due to this feature this converter is best suited for dc grid application and both input source can be utilize to fulfill load demand.

Table I Converter Circuit Element Design Equations

The design equation of the circuit element can be obtained from time domain analysis.

$L_1 = \frac{V_{g1} d_1}{f_s \Delta i_{L1}}$	$C_1 = \frac{i_{L3} d_1}{f_s \Delta v_{c1}}$
$L_2 = \frac{V_{g2} d_1}{f_s \Delta i_{L2}}$	$C_2 = \frac{I_0 (d_2 - d_1)}{f_s \Delta v_{c2}}$
$L_3 = \frac{V_0 (1-d_1)}{f_s \Delta i_{L3}}$	

For the proposed converter assuming inductor current ripple to be 10% of current and capacitor voltage ripple to be 5% of output voltage. From Table I.

L_1=312 µH, L_2=513 µH, L_3=702 µH

C_1=27 µF, C_2=60 µF.

From equation 1 system matrices in the corresponding mode can be written as,

$$A_1 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & -\frac{r_2}{L_2} & 0 & 0 & 0 \\ 0 & 0 & -\left(\frac{r_{c1}+r_3}{L_3}\right) & \frac{1}{L_3} & 0 \\ 0 & 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\left(\frac{1}{C_2(r_{c2}+R)}\right) \end{bmatrix}$$

(3a)

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$$P_1 = P_2 = P_3 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \quad (3b)$$

$$E_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & \dfrac{R}{R + r_{c2}} \end{bmatrix} \quad (3c)$$

$$F_1 = F_2 = F_3 = [0] \quad (3d)$$

$$B_1 = B_2 = B_3 = \begin{bmatrix} \dfrac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & \dfrac{1}{L_2} & 0 & 0 & 0 \end{bmatrix}^T \quad (3e)$$

$$A_2 = \begin{bmatrix} -\left[\dfrac{r_1 + r_{c1}}{L_1}\right] & 0 & \dfrac{r_{c1}}{L_1} & -\dfrac{1}{L_1} & 0 \\ 0 & -\dfrac{r_2}{L_2} & 0 & 0 & 0 \\ \dfrac{r_{c1}}{L_3} & 0 & -\dfrac{r_{c1} + r_3}{L_3} & \dfrac{1}{L_3} & 0 \\ \dfrac{1}{C_1} & 0 & -\dfrac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\left(\dfrac{1}{C_2(r_{c2} + R)}\right) \end{bmatrix} \quad (3f)$$

$$E_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & \left(\dfrac{R}{R + r_{c2}}\right) \end{bmatrix} \quad (3g)$$

$$A_3 = \begin{bmatrix} -\left(\dfrac{r_1 + r_{c1}}{L_1}\right) & -\left(\dfrac{r_{c1}}{L_1}\right) & 0 & -\dfrac{1}{L_1} & 0 \\ -\dfrac{r_{c1}}{L_2} & -\dfrac{R_p}{L_2} & -\dfrac{R_e r_{c2}}{L_2} & -\dfrac{1}{L_2} & -\dfrac{R_e}{L_2} \\ 0 & -\dfrac{R_e r_{c2}}{L_3} & -\dfrac{1}{L_3}\left(r_3 + R_e r_{c2}\right) & 0 & -\dfrac{R_e}{L_3} \\ \dfrac{1}{C_1} & \dfrac{1}{C_1} & 0 & 0 & 0 \\ 0 & \dfrac{R_e}{C_2} & \dfrac{R_e}{C_2} & 0 & -\left(\dfrac{R_m}{C_2}\right) \end{bmatrix}$$

Where,

$$R_e = \frac{R}{R + r_{c2}} \quad R_m = \frac{1}{R + r_{c2}} \quad R_p = r_2 + r_{c1} + R_e r_{c2} \quad E_3 = \begin{bmatrix} 0 & \dfrac{Rr_{c2}}{(R + r_{c2})} & \dfrac{Rr_{c2}}{(R + r_{c2})} & 0 & \dfrac{R}{(R + r_{c2})} \end{bmatrix} \quad (3j)$$

The small-signal discrete-time model [4] can be written as:

$$\hat{x}[n] = \phi \hat{x}[n-1] + \gamma_1 \hat{d}_1[n-1] + \gamma_2 \hat{d}_2[n-1] \quad (4)$$

The output state-space equation can be written as follows:

$$\hat{y}[n] = E_i \hat{x}[n]. \quad (5)$$

In dc-dc converters discrete time modeling can be easily established for trailing edge and leading edge modulation In this paper, trailing-edge OFF-time sampling with a sampling frequency $f_s(=1/T_s)$, as shown in Fig. 5, is implemented. In trialling edge off time

sampling the signal is sensed during off time, and the PWM pulses are aligned at the beginning of the pulse. The mathematical analysis is discussed in the following paragraphs. From Fig. 2 in interval-1, $(n-1)T_s < t < [(n-1)T_s + t_d - d_1 T_s]$ the system state equation can easily be written as

$$\dot{x} = A_3 x \qquad (6)$$

Assuming the source voltage is almost constant during each mode of operation of the switching cycle, the discrete-time model with state 'x[(n-1)T_s]' at the beginning [4] and duty ratio 'd' can easily be defined by

$$x[(n-1)T_s + t_d - d_1 T_s] = e^{A_3(t_d - d_1 T_s)} x[(n-1)T_s] \qquad (7)$$

Along similar lines, the discrete-time models for the remaining time intervals are established as

Iinterval-2: $[(n-1)T_s + t_d - d_1 T_s] < t < [(n-1)T_s + t_d]$

$$x[(n-1)T_s + t_d] = e^{A_1[d_1 T_s]} e^{A_3(t_d - d_1 T_s)} x[(n-1)T_s + t_d - d_1 T_s] \qquad (8)$$

Interval-3: $[(n-1)T_s + t_d] < t < [(n-1)T_s + t_d + (d_2 T_s - d_1 T_s)]$

$$x[(n-1)Ts + td + (d_2 T_s - d_1 T_s)] = e^{A_2[d_2 T_s - d_1 T_s]} e^{A_1 d_1 T_s} e^{A_3(t_d - d_1 T_s)} x[(n-1)T_s] + K_1 T_s e^{A_2 T_s [d_2 - d_1]} \hat{d}_1(n-1) \qquad (9)$$

Interval 4: $[(n-1)T_s + t_d + (d_2 T_s - d_1 T_s)] < t < [nT_s]$

$$x[nT_s] = e^{A_3[T_s - d_2 T_s - t_d + d_1 T_s]} e^{A_3[t_d - d_1 T_s]} e^{A_2 T_s (d_2 - d_1)} e^{A d_1 T_s} x[(n-1)T_s] + K_1 T_s e^{A_3[T_s - d_2 T_s - t_d + d_1 T_s]} e^{A_2 T_s [d_2 - d_1]} \hat{d}_1(n-1) + K_2 T_s e^{A_3[T_s - d_2 T_s - t_d + d_1 T_s]} \hat{d}_2(n-1) \qquad (10)$$

The small-signal discrete-time model in standard form for the converter under discussion can be written as:

$$\hat{x}[nT_s] = \phi \hat{x}[(n-1)T_s] + \gamma_2 \hat{d}_2[(n-1)T_s] + \gamma_1 \hat{d}_1[(n-1)T_s] \qquad (11)$$

Comparing eqns. (10) & (11), it is easy to obtain

$$\phi = e^{AT_s}, \quad \gamma_1 = K_1 T_s e^{A_3[T_s - d_2 T_s - t_d + d_1 T_s]} e^{A_2 T_s [d_2 - d_1]}$$

$$\gamma_2 = K_2 T_s e^{A_3[T_s - d_2 T_s - t_d + d_1 T_s]} \quad K_1 = [(A_1 - A_2)x + (B_1 - B_2)U]$$

$$K_2 = [(A_2 - A_3)x + (B_2 - B_3)U].$$

Taking the z-transform of eqn. (11),

$$x(z) = [zI - \phi]^{-1} [\gamma_1 d_1(z) + \gamma_2 d_2(z)] \qquad (12)$$

Taking the z-transform of equation (8) results in

$$y(z) = E_i x(z) \qquad (13)$$

Combining eqns. (9) and (10) results in

$$y(z) = E_i [zI - \phi]^{-1} \gamma_2 d_2(z) + E_i [zI - \phi]^{-1} \gamma_1 d_1(z). \qquad (14)$$

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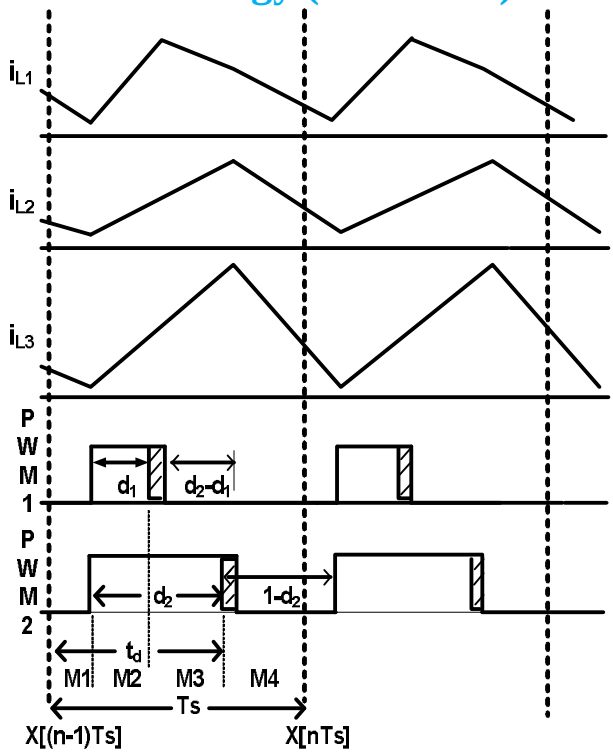

Fig. 5. PWM gating signals and Off-Time sampling process.

III. APPLICATION OF RGA THEORY TO CONVERTER

To design the controller for two input converter we need to know the degree of interaction between the control loops. The most popular method of interaction analysis is Relative Gain Array RGA .From this analysis we can decide the best suited control signal to control output voltage and source current.RGA is the ratio of open loop gain to closed loop gain. For the proposed converter interaction is less so decentralized controller is preferred. Expression of RGA may be defined as.

$$\wedge(G) = G(0).*(G(0)^{-1})^{T} \qquad (15)$$

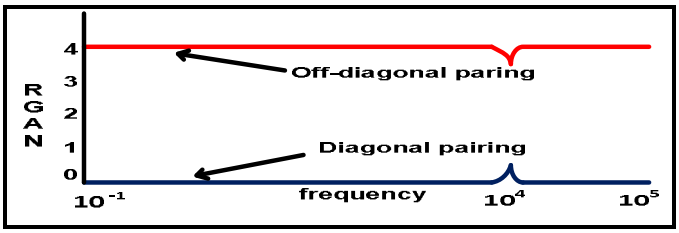

Fig. 6.RGAN v/s frequency plot

$$RGA = \begin{bmatrix} 1.0004 & -0.0004 \\ -0.0004 & 1.0004 \end{bmatrix}$$

IV. SIMULATION STUDIES AND EXPERIMENTAL RESULTS

To study the salient features of proposed two input DC-DC converter and to verify the dc bus regulation together with the load distribution capability a 48 V, 177 Watts converter is considered. In this converter DC source-1 is a low voltage source and DC source -2 is considered as high voltage source. The parameters of the converter element is shown in Table-I. For the parameters given by Table 1 transfer functions of this converter are.

$$G_{11}(z) = \frac{-1.05z^4 + 4.829z^3 - 8.173z^2 + 6.08z - 1.685}{den}$$

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$$G_{12}(z)=\frac{0.3685z^4-1.24z^3+1.528z^2-0.8085z+0.1522}{den}$$

$$G_{21}(z)=\frac{-0.02209z^4+0.07044z^3-0.08246z^2+0.04166z-0.007567}{den}\quad G_{22}(z)=\frac{2.393z^4-9.236z^3+13.4z^2-8.657z+2.103}{den}$$

$$den=z^5-4.883z^4+9.567z^3-9.403z^2+4.636z-0.9172 \quad (16)$$

For this converter PSIM is used for simulation purpose steady state voltage and inductor current waveform are shown in figure 8 and 9 respectively .Load shared by each source is show in figure 10.

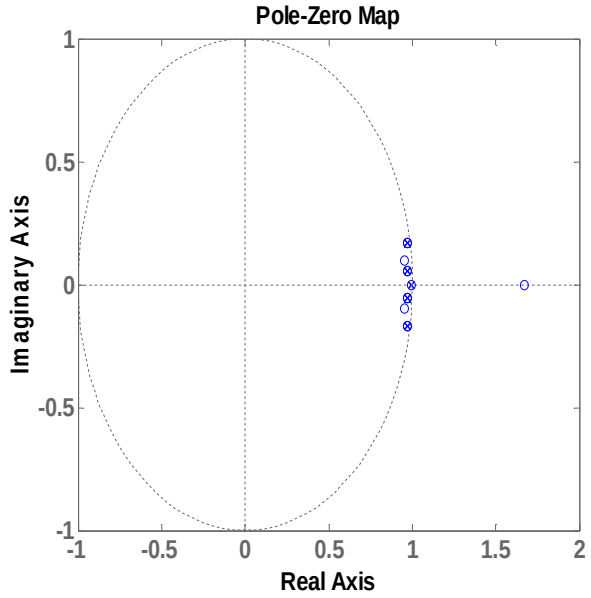

Fig. 7Polee zero plot of the transfer function (G)

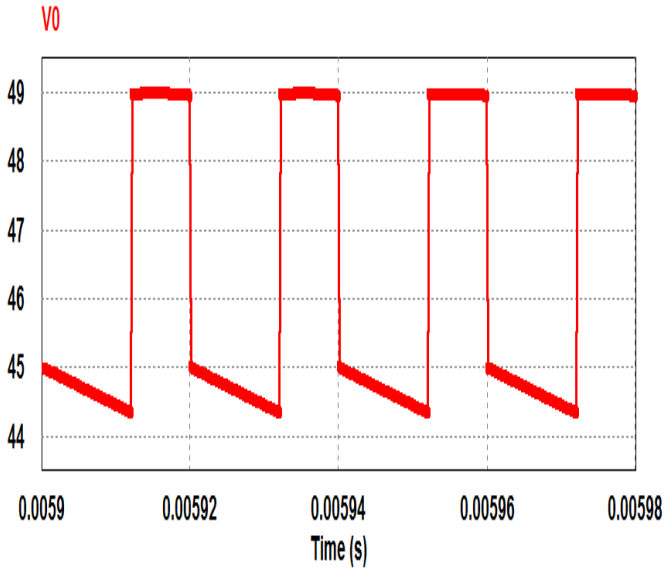

Fig. 8.steady state waveform of load voltage

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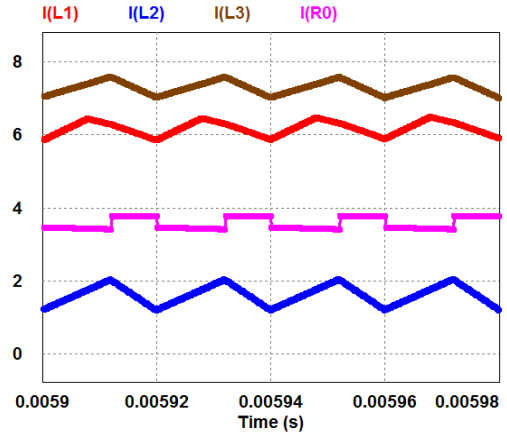

Fig. 9.steady state waveform of inductor and load current

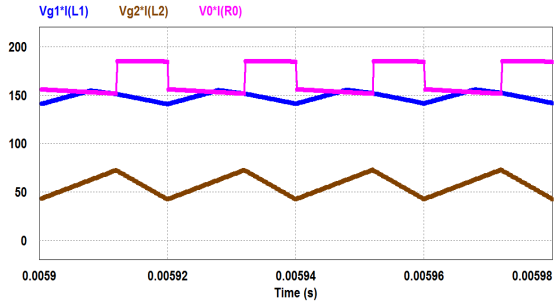

Fig. 10 .Load power distribution

V. CONCLUSION

A new two input boosting DC-DC converter for dc grid application is proposed in this paper. State space and discrete time modeling have been performed for different mode of operation, Simulation results were in agreement with theoretical studies.

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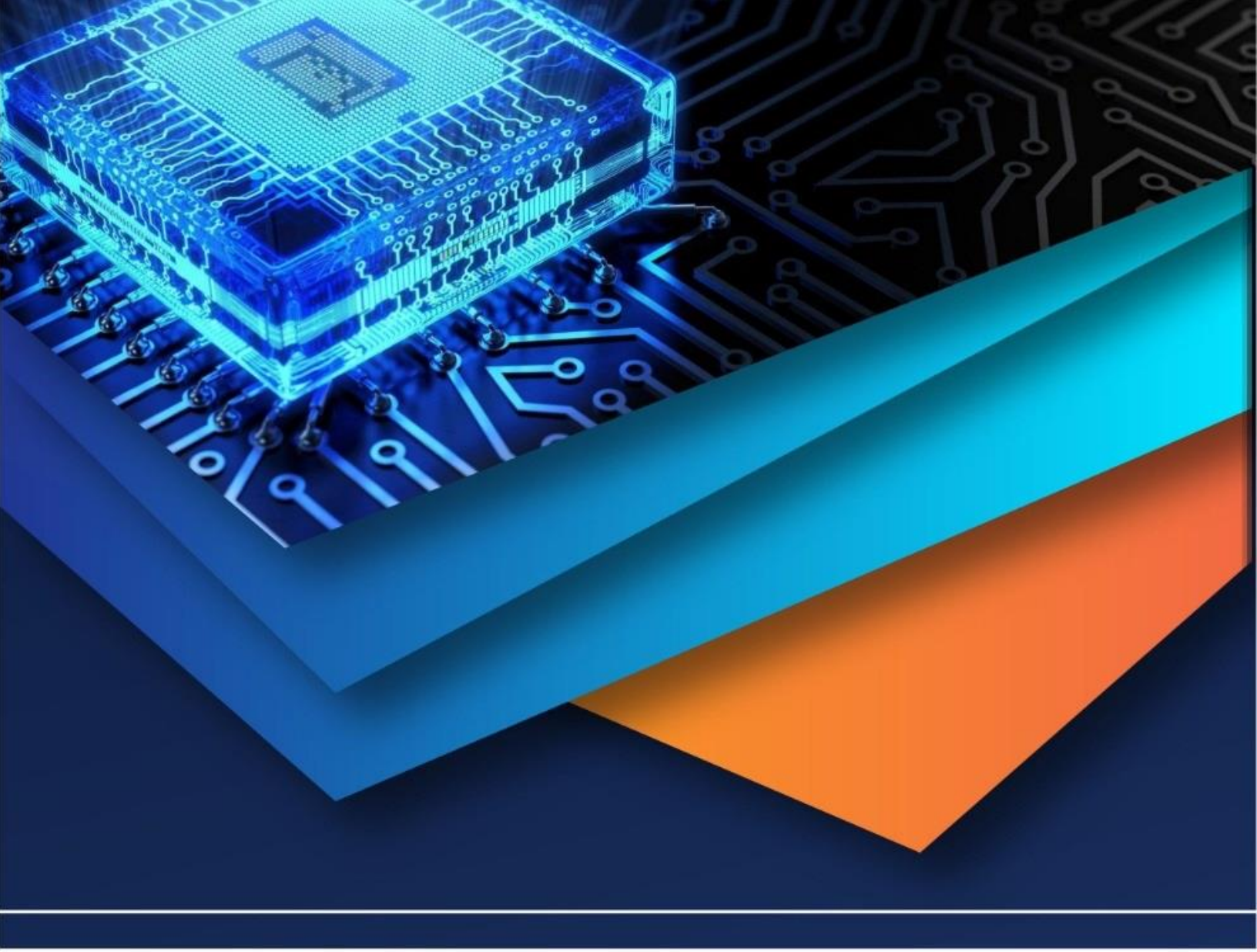

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