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FPGA Implementation OF Reed Solomon Encoder and Decoder

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Abstract: *Advanced communication techniques along with accuracy of information being very critical, the use of traditional Forward Error Correction (FEC) methods has become widespread. FEC provides a significant improvement to the system in terms of reliability of data reception. The basic principle behind error-correcting codes is the application of a mathematical transform onto the message signal such that redundant message information is used to correct any errors that may have been introduced during transmission. Reed Solomon Encoder and Decoder falls in the category of forward error correction encoders and it is optimized for burst errors rather than bit errors. Reed Solomon Encoder and Decoder provide a compromise between efficiency and complexity, so that this can be easily implemented using hardware or FPGA. FEC gives the receiver the ability to correct errors without needing a reverse channel to request retransmission of data, but at the cost of a fixed, higher forward channel bandwidth. FEC is therefore applied in situations where retransmissions are costly or impossible.*

Keywords-Forward Error Correction, FPGA, Reed Solomon Code.

I.INTRODUCTION

Wireless technology is fast becoming a trend in present communication systems, as the demand for greater bandwidth allocation is being addressed by fixed wireless broadband access. However, the use of free space, as a medium, introduces many sources of error in the transmission of data across the channel. Burst Error (contiguous errors in the bit stream) is a common occurrence in digital communication systems, broadcasting systems and digital storage devices. Forward error correction is a technique in which redundant information is added to the original message, so that some errors can be corrected at the receiver, using the added redundant information. Reed Solomon Encoder and Decoder falls in the category of forward error correction encoders and it is optimized for burst errors rather than bit errors.

Reed Solomon is an error correcting code capable of dealing with correcting burst errors, in mass storage devices, wireless and mobile communications units, digital television, digital video broadcasting and broadband modems. R-S codes are maximum distance separable codes, known to be the most powerful linear codes for their class, and have the ability to

correct both errors and erasures. For a typical transmission channel the addition of R-S coding allows the system to operate within approximately 4 dB of the Shannon capacity. The resulting benefit translates into higher data rates, lower bit-error rates (BERs), greater transmission distance, and greater immunity to interference effects R-S codes can be implemented on a number of platforms, traditionally being Application Specific Integrated Circuits (ASICs), then shifting toward DSPs and Programmable Logic devices (PLDs).

FPGAs provide the advantage of design reuse, faster design time especially for prototyping. A selection of the most suitable FEC to be used with the system may be provided using the benefit of the reprogrammability of FPGAs. Parallel realization of equations is possible to meet time speed constraints. Equations with multipliers and power/inversion circuits may be mapped into the look-up table architecture of the FPGAs.

This project thus aims at design and FPGA implementation of a FEC Decoder and Encoder based on Reed Solomon Codes. Coding is done in verilog for

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Syndrome Calculator, Berlekamp Massey, Forney and Chien Algorithm and encoder.

II. LITERATURE SURVEY

Till now papers are published based on the different architectures of RS decoder. A clear survey was done for recent technical research on the problem arising in the complexity of RS Decoder designing. Detailed analysis has been made to know how the encoder can be transformed such that its implementation can make use of existing decoder circuitry, requiring only little additional hardware dedicated to the encoder.

III. PROPOSED SYSTEM

The proposed system aims at designing and implementing an error detection and correction system using Reed Solomon encoder and decoder.

The generating polynomial for an R-S code is driven as:

$$g(x) = g_0 + g_1x + g_2x^2 + \dots + g_{2t-1}x^{2t-1} + x^{2t} \quad (1)$$

With degree equal to the number of parity symbols (n-k). Since the generator polynomial of degree n-k, there must be precisely n-k successive powers of α that are roots of the polynomial.

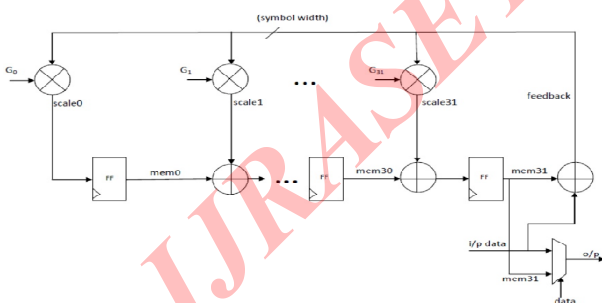


Fig 1: Reed Solomon encoder block diagram

By shifting a message polynomial $m(X)$, which is to be encoded into the rightmost k stages of a codeword register, and then appending a parity polynomial, $p(X)$ by placing it in the leftmost $n-k$ stages. Then, multiplying $m(X)$ by x^{n-k} is done to manipulate the message polynomial algebraically so

that it is right-shifted $n - k$ positions. Next, dividing $x^{n-k} m(X)$ by the generator polynomial $g(X)$, which can be written as:

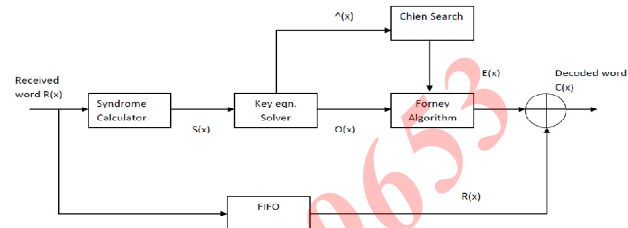
$$x^{n-k}m(x) = q(x)g(x) + p(x) \quad (2)$$


Fig 2: Reed Solomon decoder block diagram

The received codeword is entered to RS decoder to be decoded, the decoder first tries to check if this codeword is a valid codeword or not. If it does not, errors occurred during transmission. This part of the decoder processing is called error detection. If errors are detected, the decoder try to correct this error using error correction part.

1. Error detection part, in this part we use “Syndrome computation” block.
2. Error correction part, this part consists of three blocks:
 - a. Decoding algorithm which used to find the coefficients of error-location polynomial $\sigma(x)$ and error-evaluator polynomial $W(x)$ it sometimes called “Key equation solver”.
 - b. Chien search block which used to find the roots of $\sigma(x)$ which present the inverse of the error locations.
 - c. Inverse transform block which used to find the values of the errors

IV. WORK METHODOLOGY

a. Syndrome Calculator

The Syndrome calculation block treats the input codeword as a series of polynomial coefficients and calculates a syndrome polynomial of $2t$ coefficients.

Syndrome polynomial $S(x)$ formed as:

$$S(x) = \sum_{i=1}^{2t} S_i X^{i-1} \quad (3)$$

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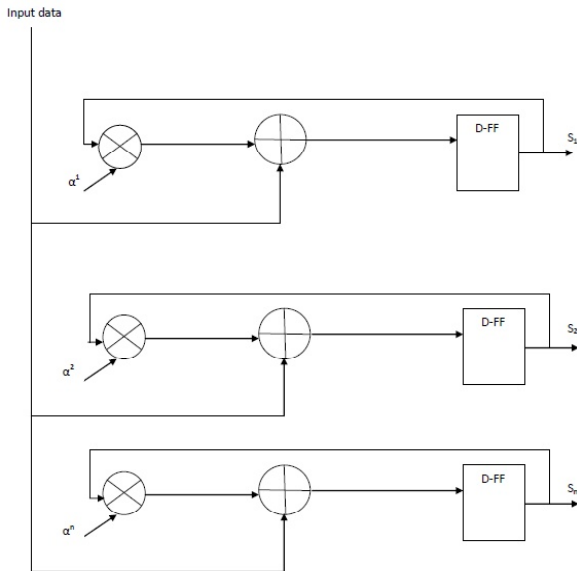


Fig 3: Block diagram of Syndrome Calculator

b. Berlekamp Algorithm

Input: Syndrome polynomial from the last slide
Output: Error Locator Polynomial $\sigma(z)$ and Error Evaluator Polynomial $\omega(z)$. Defined as:

$$\sigma(z) = \prod_{i=1}^s (1 - X_i z) \tag{5}$$

$$\omega(z) = \sigma(z) + \sum_{i=1}^s z X_i Y_i \prod_{j=1}^s (1 - X_j z) \tag{6}$$

c. Chien Search

Chien's Search takes error locator polynomial $\sigma(z)$ and outputs the error locations/positions (X_i and j_i). The output of Chien Search is the sum,

$$A = \sum_{j=1}^v \wedge_j \alpha^j = \wedge(x) - 1|_{x=\alpha}$$

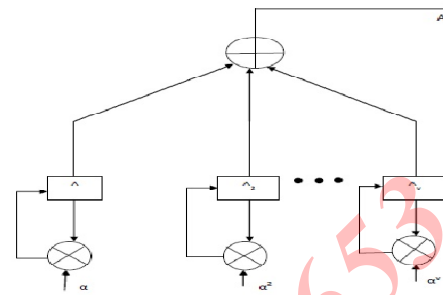


Fig 4: Block diagram of Chien Search

d. Inverse Transform and Error Correction

The final step of the decoding procedure is to compute the inverse transform

$$e^i = \sum_{l=1}^n E_l \alpha^{l(i)} \tag{7}$$

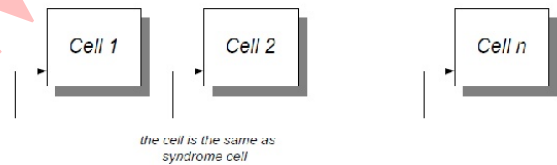


Fig 5: Block diagram of Inverse Transform Circuit

V.RESULT

Simulations of the proposed design will be conducted in the Xilinx 12.2 and modelsim. The verified Verilog code will be then downloaded on FPGA.



Fig 3: Simulation result of Encoder using Modelsim

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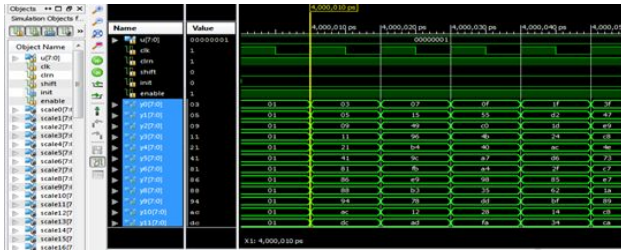


Fig 4: Simulation result of Syndrome Calculator using Modelsim

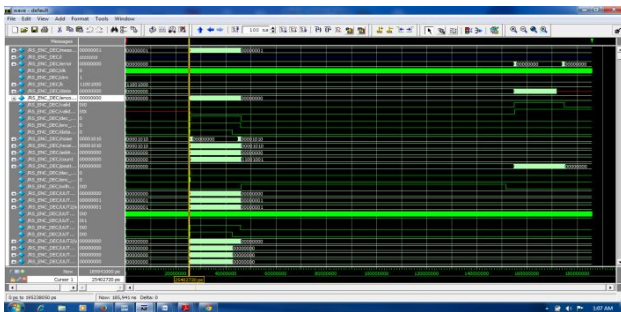


Fig 4: Simulation result of Decoder using Modelsim

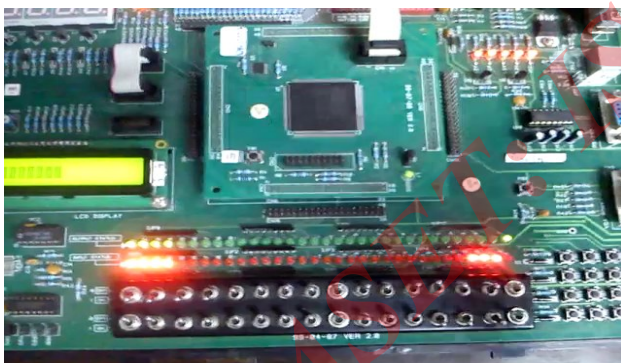


Fig 5: FPGA output for RS Encoder

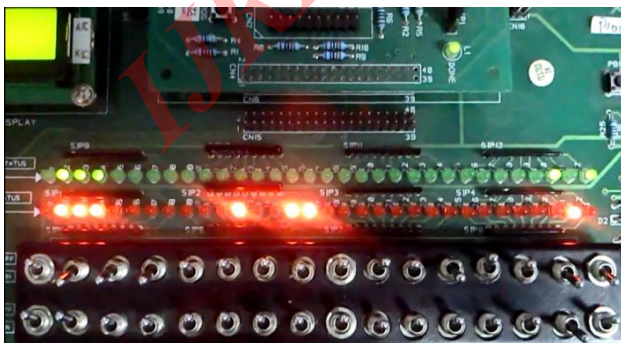


Fig 6: FPGA output for RS Decoder

VI. CONCLUSION

The main advantage of the proposed scheme is that, RS codes has less coding gain as compared to LDPC and turbo codes. But it has very high coding rate and low complexity. Hence it is suitable for many applications including storage and transmission. Berlekamp algorithm gives the maximum throughput compared to Euclidean algorithm.

In future design can be still made robust by implementing further advanced key equation mechanism to improve the error detection and correction capability. Area can also be effectively reduced in the process.

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