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Fault Current Limitation in a Power System Network by Using SFCL through Step Input Approach

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Abstract: Power system networks are growing day by day and its attributes are changing rapidly. The continuous increase in the interconnection of various power grids to form a central grid and the growing power demand has led to an increase in fault current levels. This increase in the fault current has led to a simultaneous increase in the current interrupted by the circuit breaker also which makes it to break fault currents which are out of its rated breaking capacity. This paper utilizes a resistive model of a superconducting fault current limiter (SFCL) modelled in Simulink environment of MATLAB to mitigate this problem. The current limiting effect is achieved by an almost immediate transition of the HTS material from the superconducting state to a normal resistive state. A power system network is modelled and fault currents are observed with and without the SFCL model. Graphical simulations are also presented to show the effectiveness of the proposed model and the percentage reduction in fault current levels is also shown.

Keywords: Fault current, SFCL, Superconducting fault current limiter, Resistive SFCL, MATLAB Simulink/Simpower system.

I. INTRODUCTION

Due to continuous addition of distributed generation, large scale interconnection of power system networks and parallel operation of transformers to improve the reliability of the network, the fault current levels in the modern day power system networks is increasing. Excessive fault currents cause stresses and lead to high electrical, mechanical and thermal instabilities of electric networks. As a consequence, the ever-increasing levels of fault current are gradually exceeding the interruption capabilities of existing devices therefore causing the installed circuit breakers to burst while interrupting currents which it is not capable of interrupting [1]. Therefore there is an urgent need to limit the fault current levels because of which the installed circuit breakers are interrupting currents out of their rated breaking capacity as a consequence of which they are bursting. Until now, many devices such as split bus bars, transformers with higher impedance, and fuses have been used in industry to reduce the peak value of fault currents. However, the use of these devices has limitations, in that they can damage the reliability of the power system or increase power loss. SFCL presents an attractive prospect in limiting the fault current very effectively without additional power losses during normal operation and at the same time improving the transient stability of the system.

When any of the critical limits defining the transition between the superconducting state to the normal state, such as critical temperature (T_c), critical current density (J_c), or critical magnetic field (H_c), is exceeded the superconducting material almost instantaneously quenches from the superconducting state to normal state and thus offers a high resistance during fault conditions[2]. Additionally the SFCL returns to its superconducting state once the fault is cleared and its application requires no change in the existing network topologies.

II. RESISTIVE SFCL MODEL

Many models of SFCL have been developed till date resistive type, reactive type, transformer type, and hybrid type SFCLs. In this paper we will focus on the resistive model of SFCL developed using MATLAB/Simulink based computer simulation.[3]

Mathematically, resistance of SFCL is expressed as given in the equations below

$$R_{sfcl}(t) = \begin{cases} 0, & t < t_0 \\ R_m [1 - \exp\left(\frac{-t+t_0(Quench)}{T_{sc}}\right)^{\frac{1}{2}}], & t_0 \leq t < t_1 \\ \alpha_1(t - t_1) + \beta_1, & t_1 \leq t < t_2 \\ \alpha_2(t - t_3) + \beta_2, & t > t_2 \end{cases}$$

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Where R_m is the maximum resistance of the SFCL in the quenching state, TSC is the time constant of the SFCL during transition from the superconducting state to the normal state. Furthermore, t_0 is the time to start the quenching. Finally, t_1 and t_2 are the first and second recovery times, respectively.

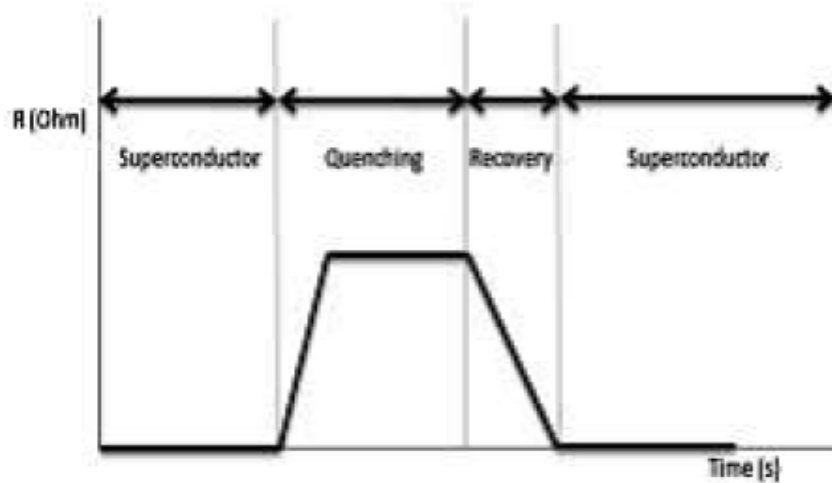


Fig. 1 SFCL behaviour characteristics

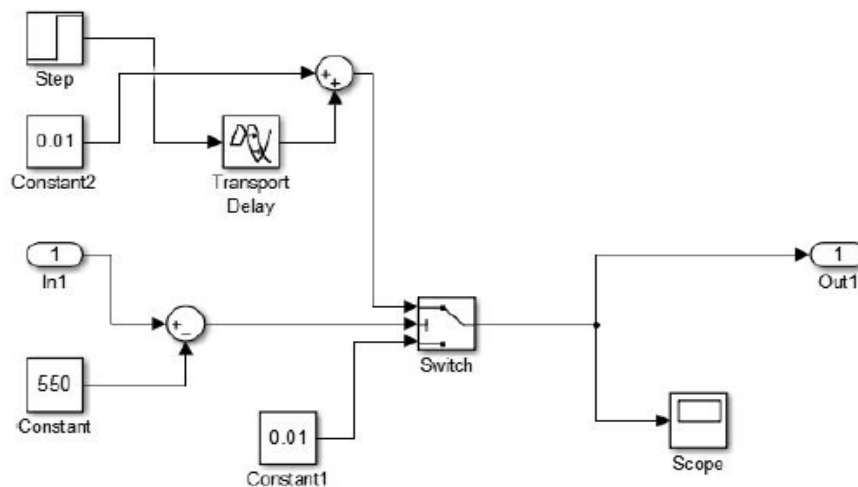


Fig. 2 SFCL model developed in Simulink

The graphical representation of the four equations is shown in Figure 1. The resistive model of SFCL modelled in MATLAB is shown in Figure 2. In the model the RMS value of the current passing through the SFCL is compared with the triggering current of the SFCL which is 550 Amperes in the model developed [4]. If the passing current is below the triggering value, the SFCL exhibits the lowest resistance state which is typically 0.01 ohms and continues to be in superconducting stage. If the current flowing is above the triggering value of current the SFCL quenches from superconducting stage to normal stage after a response time of 2ms and exhibits a maximum resistance of 20 ohms. The delay in the response is implemented using a step input block and a transport delay block which holds the step input to the system which is virtually the resistance to be offered by the SFCL for a period of 2ms. The resistance from the above model is then multiplied with the current flowing in the network to form a voltage which is filtered out using a first order filter to reduce harmonics and it is then given to a controlled voltage source to compensate for the voltage sag caused during short circuit or faulty conditions.

Table. 1 SFCL vs. Conventional Solutions

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Solutions	Advantages	Disadvantages	Relative expense
New Substation	Provides opportunity for future growth	Expensive and lengthy to install	Most expensive solution
Bus Splitting	Separates sources of fault current	Separates sources of load current from load centers and undermines system reliability	High, if split bus not already installed
Multiple Circuit Breaker Upgrades	Most direct solution with no adverse	Difficult to schedule outages; bus work reinforcement also required	High to medium, depending on number of circuit breakers
Current Limiting Reactors	Easy to install	Voltage Drop and power losses; potentially cause instability.	Medium to Low
Sequential Breaker Tripping	No major hardware Installation involved	Expands impact of fault to wider range of the system	Low

III. COMPARISON OF SFCL WITH OTHER CONVENTIONAL SOLUTIONS

Before analysing the effect of installing a SFCL in a network, the relative cost of SFCL with the other methods to reduce fault currents in a network were compared. Table I summarizes the conventional solutions and their respective pros, cons and relative cost [5]. Table I primarily considers the initial capital installation cost in the comparison. In the cases of multiple circuit breaker upgrades, the cost of bus work reinforcement must also be considered, since the level of fault current is not being reduced. This comparison reveals that the SFCL is cost competitive with most of the conventional solutions except current limiting reactors and sequential breaker tripping.

IV. POWER SYSTEM NETWORK SETUP

There are two power system networks used in this paper to study the effect of SFCL when it is used to limit the fault current [6-7]. These power system networks correspond to the present network used by a company in Mumbai, India. The company encountered the problem of some circuit breakers either bursting or operating in over duty condition due to increase in fault levels across its network due to increasing demand and increase in generators being added to meet the demand.

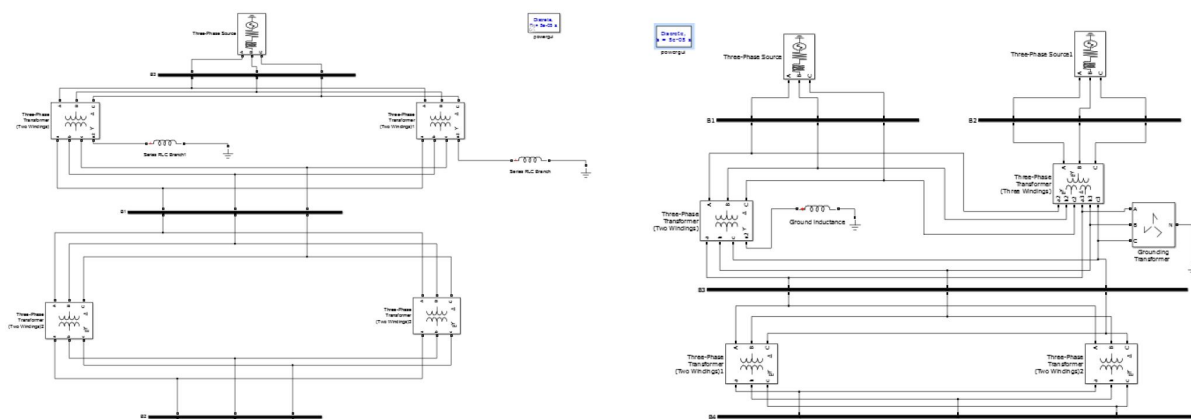


Fig. 3 Layout of Network-1 Network-2

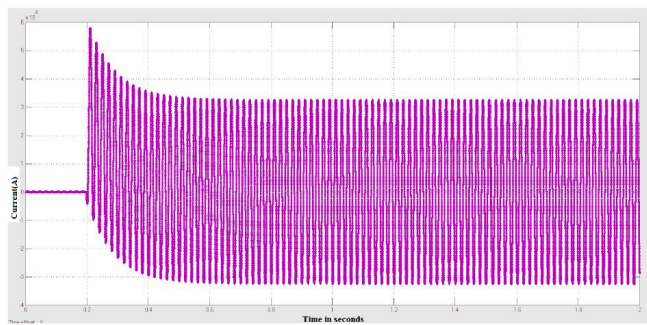
Both the networks are first modeled using Mipower and short circuit studies are conducted on both the circuits to obtain the actual fault current [8]. Then the networks were modeled in MATLAB Simulink and the SFCL model was inserted along with the modeled network and the simulation results were observed. The first network consists of an equivalent generator in place of an infinite bus whose parameters are entered using the 3-phase fault level on Bus-1. The three phase fault level on bus-1 is 5182.29MVA. The

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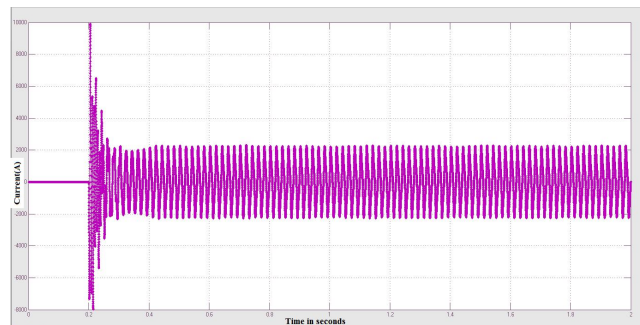
generators are followed by two 75MVA 110KV/22KV Dy11 transformers connected in parallel on Bus-2. These transformers are grounded using a reactance having the value of 1.5 ohms/phase. The voltage is again stepped down from 22KV to 11KV using two 20 MVA Dy11 transformers connected in parallel on Bus-3. There are two infinite buses which are replaced by an equivalent generator of 110KV and 220KV respectively and the values are specified using the short circuit MVA respective buses. The short circuit level on Bus-1 is 4055.66MVA and on Bus-2 is 13720.047MVA. Bus-1 and Bus 2 are interconnected using a 3 winding transformer through the secondary winding of the 3 winding transformer. A 75MVA 110KV/33KV Dyn11 transformer is connected between bus 1 and bus 3 which is grounded using a reactor of 1.5 ohms/phase. Bus 2 is connected to Bus 3 using the tertiary winding of the 3 winding transformer [9]. The 3 winding transformer is of 250/200/75 MVA, 220KV/110KV/33KV star-star-delta transformer whose tertiary winding is grounded using a zig-zag grounding transformer [10]. Bus 3 and Bus 4 are connected by two 20MVA 33KV/11KV Dy11 transformers connected in parallel. The secondary of the transformers are solidly grounded. The network is shown in figure 3.

V. SIMULATION RESULTS

Short circuit studies were conducted on the two networks using SFCL installed above Bus-2. LLL and LG fault conditions were created using Simulink and the effectiveness of installing SFCL to limit fault current was observed. Fault analysis on network-1: Figure 4(a) and (b) shows the waveform obtained for a LLL fault at bus 2 without and with SFCL respectively. Figure 5(a) and (b) shows the waveforms obtained for a LG fault at Bus 2 without and with SFCL installed respectively. Similar faults were created at bus-3 also. It can be seen that the introduction of SFCL reflects in the fault current with the fault current decreasing substantially during various faults which were simulated.

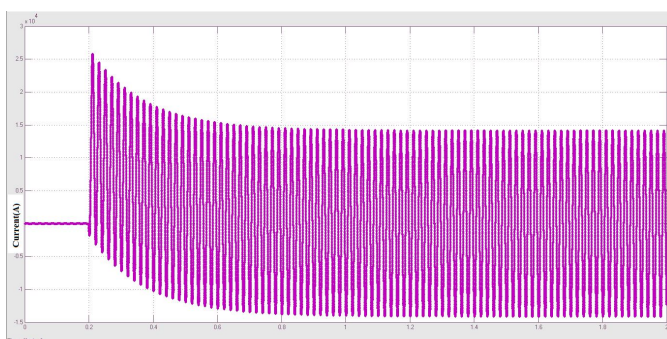


(a) LLL fault at Bus 2 without SFCL installed-22.144KA

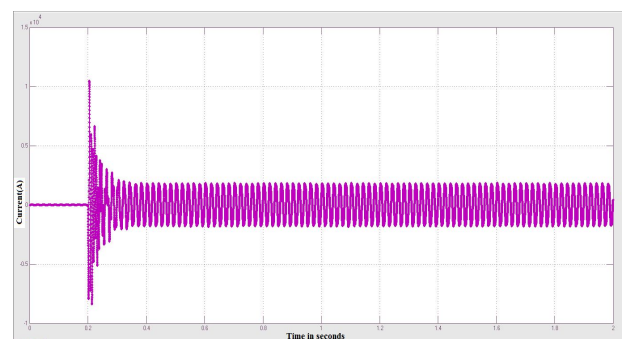


(b) LLL fault at Bus 2 with SFCL installed-4.96KA

Fig. 4 LLL fault at Bus 2 without SFCL installed-22.144KA and LLL fault at Bus 2 with SFCL installed-4.96KA



(a) LG fault at Bus 2 without SFCL installed-9.771KA



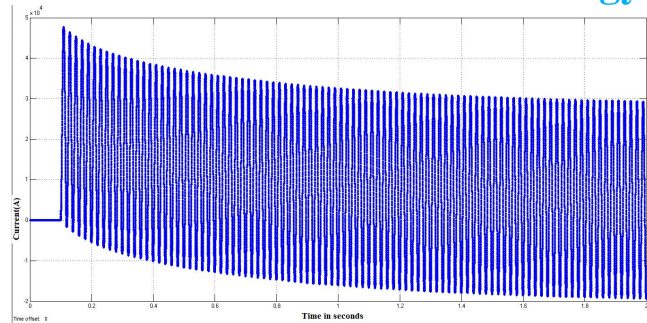
(b) LG fault at Bus 2 with SFCL installed-4.77KA

Fig. 5 LG fault at Bus 2 without SFCL installed-9.771KA and LG fault at Bus 2 with SFCL installed-4.77KA

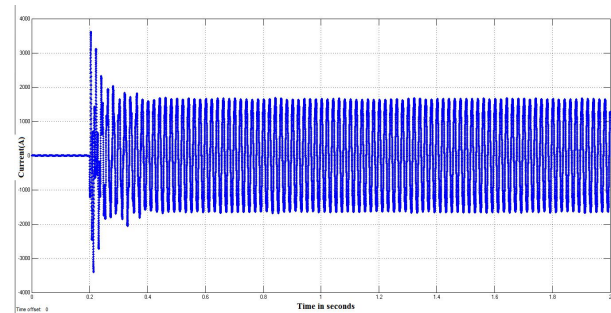
Fault analysis on network-2: The zig zag grounding transformer used to ground the delta winding of the 3 winding transformer blocks positive and negative sequence currents and allows only zero sequence currents to flow through it during unbalanced fault conditions.

Figure 6 (a) and (b) shows the waveforms obtained for a LLL fault on bus-3 without and with SFCL installed respectively. Figure 7 (a) and (b) shows the waveforms obtained for a LG fault on bus-3 without and with SFCL installed respectively. Similar faults were created at bus 4 also.

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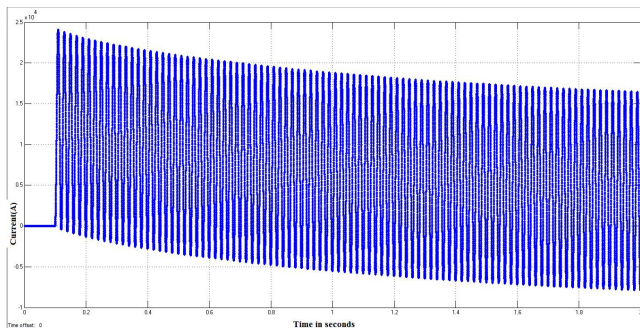


(a) LLL fault at Bus 3 without SFCL installed-16.627KA

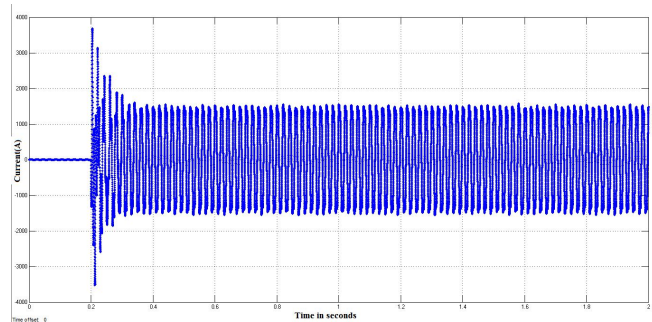


(b) LLL fault at Bus 3 with SFCL installed-5.47KA

Fig. 6 LLL fault at Bus 3 without SFCL installed-16.627KA and LLL fault at Bus 3 with SFCL installed-5.47KA



(a) LG fault at Bus 3 without SFCL installed-8.443KA



(b) LG fault at Bus 3 with SFCL installed-4.94KA

Fig. 7 LG fault at Bus 3 without SFCL installed-8.443KA and LG fault at Bus 3 with SFCL installed-4.94KA

The results which are summarized in Table-II and Table-III shows the dominant effect of SFCL when it is introduced in the network to reduce the fault current. The fault currents get reduced by a substantial margin thus allowing the circuit breakers to operate well within their duty.

VI. CONCLUSION

This paper conducted short circuit studies on two of the practical network topologies used by a Generation and Trans-mission Company in Mumbai, India and the effect on fault current after installing an SFCL on such a network was observed. The Superconducting Fault Current Limiter is a promising device to limit the escalating fault levels caused by the expansion of power grid and integration of renewables. It was shown from the results that the resistive SFCL is very effective in reducing the level of short circuit current quasi instantaneously. Therefore the reliability and stability of power system can be improved by the application of SFCL.

However, the optimal location of SFCL in a large scale power system is a matter of further research. The protection co-ordination problem of the SFCL with other protective devices installed is another one of the remaining questions which needs to be answered in future. In other words, existing protective devices such as a recloser, may not be operated correctly when the fault current level is very low by the damping that the SFCL can provide.

REFERENCES

- [1] Apurbo Biswas, Md. Elias khan and Utpal sarker, "Transient Stability Improvement of a Conventional Power System by Superconducting Fault Current Limiter," Global Journal of Researches in Engineering Electrical and Electronics Engineering, Volume 13 Issue 5 Version 1.0 Year 2013.
- [2] Byung Chul Sung, Dong Keun Park, Jung-Wook Park, and Tae Kuk Ko, "Study on a Series Resistive SFCL to Improve Power System Transient Stability: Modeling, Simulation, and Experimental Verification," IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 56, NO. 7, JULY 2009.
- [3] X. Zhang, H. S. Ruiz, Z. Zhong, and T. A. Coombs, "Implementation of Resistive Type Superconducting Fault Current Limiters in Electrical Grids: Performance Analysis and Measuring of Optimal Locations," arXiv:1508.01162v1 [cond-mat.supr-con] 4 Aug 2015.
- [4] Ming-Tang Chen and Chi-Hung Nguyen, "Voltage quality performance improvement of a distribution feeder with Superconducting Fault Current Limiter," International Journal on Electrical Engineering and Informatics Volume 7, Number 1, March 2015.
- [5] G. Vijaya Kumar, J. Prakash Kumar, "VIABLE SYSTEM PHENOM-ENA OF SFCL AND PROTECTIVE COORDINATION FOR SMART GRID APPLICATIONS," [IJESAT] INTERNATIONAL JOURNAL OF ENGINEERING SCIENCE AND ADVANCED TECHNOLOGY, Volume-2, Issue-5,

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

1528 1533.

- [6] Umer A. Khan, J. K. Seong, S. H. Lee, S. H. Lim, and B. W. Lee, "Feasibility Analysis of the Positioning of Superconducting Fault Current Limiters for the Smart Grid Application Using Simulink and SimPowerSystem," IEEE TRANSACTIONS ON APPLIED SUPER-CONDUCTIVITY, VOL. 21, NO. 3, JUNE 2011.
- [7] S.Vasudevamurthy 1, Ashwini.V, "Performance of a 3.3kV Resistive type Superconducting Fault Current Limiter," INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES AND RESEARCH TECHNOLOGY, June, 2014.
- [8] Priyanka Mahajan, Dr.P.J.Shah, "Designing and Analysis of Power System with SFCL Module," International Journal on Recent and Innovation Trends in Computing and Communication, Volume: 3 Issue: 2.
- [9] J.-C. Llabes, D. W. Hazelton, C. S. Weber, "Recovery under load performance of 2nd generation HTS superconducting fault current limiter for electric power transmission lines," IEEE Transactions on Applied Superconductivity, vol. 19, p. 1968, 2009.
- [10] L. Wang, P. Jiang and D. Wang, "Summary of Superconducting Fault Current Limiter Technology," Frontiers in Computer education, Springer-Verlag Berlin, Germany Heidelberg, AISC 133, pp. 819-825, 2012.



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