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# Design and FPGA Implementation of DDR SDRAM Controller

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***Abstract***: ***Technology is increasing day by day. The world is obsessed with smart phones, laptops and computers. RAM which is used in these devices is the internal memory of CPU for storing data, program and program result. SDRAM or Synchronous Dynamic Random Access Memory is able to work efficiently. It is synchronised with the clock of the processor. The advance version of SDRAM is DDR (Double Data Rate) SDRAM which transfer data on both rising and falling edges of the clock resulting in double data transfer rate. In this paper, DDR SDRAM controller is designed and implemented on FPGA. Transfer rate is 266 M bits/s/pin and clock frequency is 133 MHz This has been done using Verilog HDL on Xilinx ISE 14.2 and finally the controller is targeted to Xilinx Spartan 3E FPGA kit.***
***Keywords***: ***DDR SDRAM Controller, FPGA, Read, Write, Precharge, Burst.***

## I. INTRODUCTION

Computer memory is the storage space where data processing and instructions are stored. From toys to satellite for navigation systems, every appliance almost use high speed and high throughput memory to function. The SD RAM fetches twice the data for a single clock cycle which increases speed as well as throughput. The memory is divided into number of small parts called a cell. Each cell has a unique address. If a computer has memory of 64k then it will have 64k (64*1024) memory locations. The address of these locations will vary from 0 to 65535. [1]

Physically, RAM is made up of small electronic chips mounted on modules. There are 2 types of RAM: (a)Static(SRAM) and (b) Dynamic(DRAM). The use of Dynamic RAM is useful since memory density is increased and power consumption and area is reduced. DRAM is an array of memory cells. Compared to the structural design of SRAM, additional memory cells are packed into the memory by DRAM architecture.

In terms of speed, SRAM is faster. DRAM requires refreshing thousands of times per second in order to maintain the data while SRAM does not need refreshing, which is what makes it faster than DRAM. DRAMs memory cells are composed of capacitor and transistor. DRAM supports access times of about 60 nanoseconds, while static RAM can give access times as low as 10 nanoseconds. [2]

Double Data Rate-Synchronous DRAM, a type of DRAM that transfers the data on both the rising and falling edges of each clock cycle, doubling the memory chip's data throughput. DDR-SDRAM also consumes less power, making it suitable to notebook computers. The basic DDR SDRAM is also called DDR1_SDRAM. DDR SDRAM has the advantage of high speed and large capacity, various time latencies decrease the data transmission efficiency of DDR SDRAM greatly.

While the motherboards which are intended to employ DDR are similar to those that use SDRAM, but they are not backward compatible with SDRAM. Similarly, SDRAM motherboards are not compatible with DDR. [2 - 5]

There are burst oriented read and write accesses to the DDR SDRAM; access start at a selected location and continue for a programmed number of locations in a programmed sequence. Beginning with the registration of an ACTIVE command, access is then followed by a READ or WRITE command. Programmable read or write burst lengths of 2, 4, or 8 are provided by DDR SDRAM. To provide a self-timed row precharge that is initiated at the end of the burst access, an Auto-Precharge function is provided. [5]

## II. OPERATIONS

### *A. Burst Read Operation*

The burst read operation in DDR SDRAM is performed in the same manner as the SDRAM. The read command is given the beginning column and row address and auto precharge is either enabled or disabled for that burst. If auto-precharge is enabled, at the completion of the burst the row is precharged. Throughout read bursts, the valid data-out component from the beginning column

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address are available following the CAS latency after the read command each subsequent data-out component will be valid nominally at following positive or negative clock edgeDQS is driven by the DDR SDRAM alongside output data. The initial DQS LOW state is termed as the read preamble; the DQS LOW state coincident with the last data out component is termed as the read postamble.

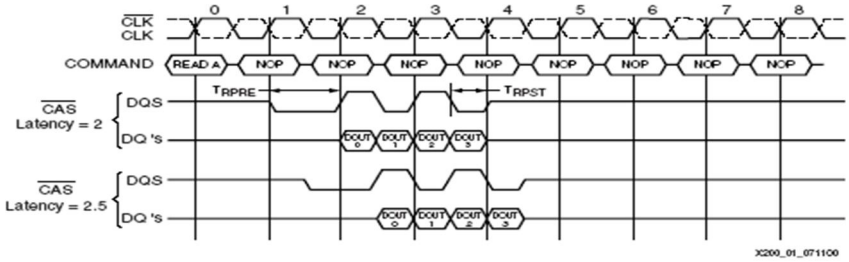


Fig. 2.1: Burst Read Operation

*B. Burst Write Operation*

The burst write operations are initiated with a WRITE command. The beginning column and bank addresses are supplied with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto-precharge is enabled, the row being accessed is precharged at the completion of the burst. throughout WRITE bursts, the primary valid data-in component is registered on the primary rising edge of DQS following the WRITE command, and subsequent data components will be registered on consecutive edges of DQS. The DQS LOW state between the WRITE command and the initial rising edge is termed as the write preamble; the DQS LOW state following the last data-in component is termed as the write postamble. [7]

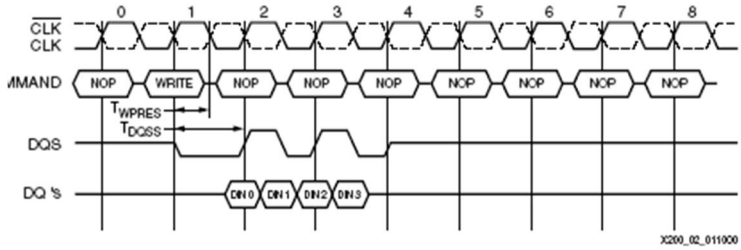


Fig 2.2: Burst Write Operation

*C. Top Level Block Diagram*

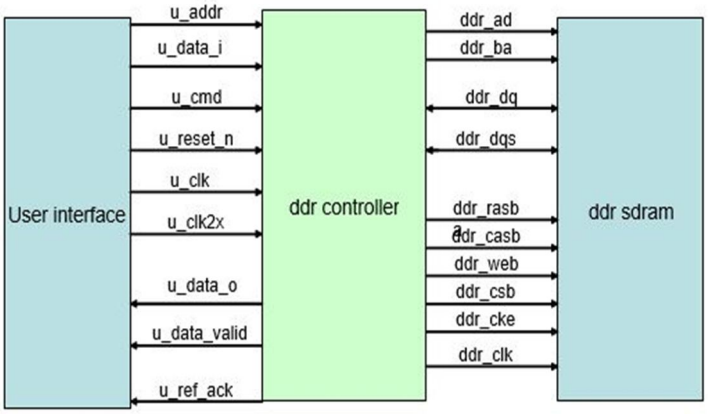


Fig 2.3: Block Diagram of DDR Controller with user interface

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*D. Controller State Machine*

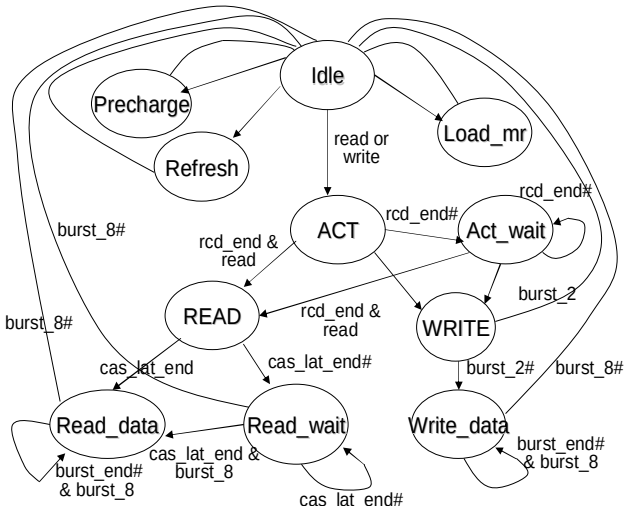


Fig 2.4: State Machine Diagram

## III. COMMANDS

The commands that would be issued by the user to the DDR SDRAM Controller.

*A. No Operation (Nop)*

The NOP command instruct the selected DDR SDRAM to perform No Operation. Unwanted commands are prevented from being registered during idle or wait states. Already progressive operations are not affected.

*B. Mode Register*

Inputs A0 to A11 load the mode registers. The load command can only be registered when all banks are idle and simultaneously another command cannot be issued. [8]

*C. Active*

To activate a row in a particular bank address, Active command is used. For bank selection B0 and B1 are used and A0-A11 selects the row address. This row remains active for accesses until a precharge command is issued to that bank. [9]

*D. Read*

The Read command is used to initiate a burst read access to an active row. The B0, B1 inputs selects the bank, and inputs A0-A7 selects the starting column. If auto precharge (A10) is selected, the row will be precharged at the end of the READ burst, else the row will remain open for subsequent accesses. [10]

*E. Write*

The Write command initiates a burst write access to an active row. The inputs B0, B1 select the bank, and the address provided on inputs A0-A7 selects the starting column. If auto precharge is selected (from A10), at the end of the burst, the row will be precharged, else the row will remain open for subsequent accesses. Input data on the DQS is written to the memory array according to the DM input logic level appearing coincident with the data. If a LOW DM signal is registered, the memory is written with the corresponding data, else the corresponding data inputs will be ignored, and WRITE will not be executed to that location. [12]

*F. Precharge & Auto-Precharge*

The precharge command is used for deactivating an open row in a particular bank or in all the banks. Input A10 determines the banks to be precharged, inputs B0, B1 select the bank. After a bank has been precharged, it remains in the idle state and must be activated prior to any command being issued. A precharge command will be treated as a NOP if there is no open row. The Auto Precharge feature performs the same precharge function described above, but without requiring an explicit command. It is accomplished from A8 bit to enable auto precharge in conjunction with a specific command(R/W). [13-14]

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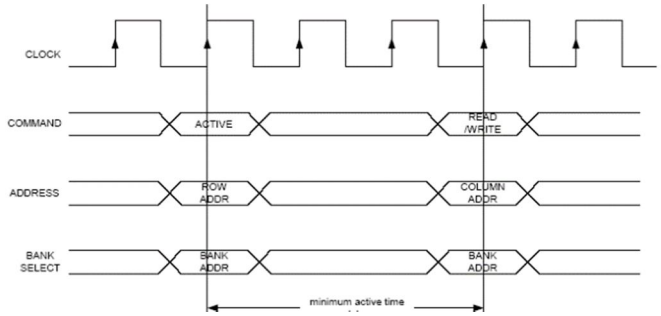


Fig. 3.1: Minimum Active Timing.

## IV. SIMULATIONS & RESULTS

The Proposed design is simulated on iSim 14.2 and synthesized on Xilinx ISE 14.2 and then finally targeted to the Xilinx Spartan 3 FPGA device. The simulations, RTL Schematic and synthesis summary is shown below.

### *A. RTL Schematic*

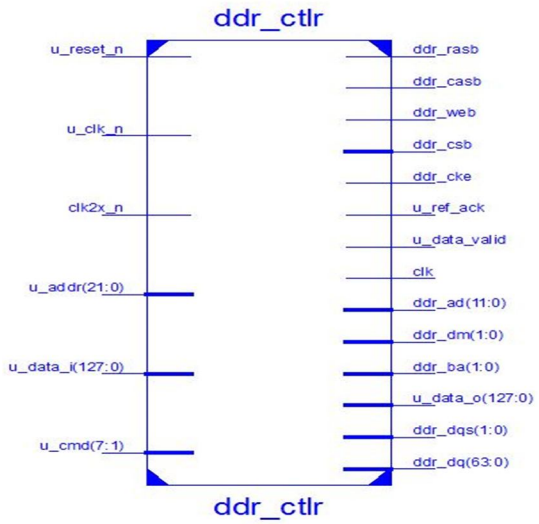


Fig 4.1: RTL Schematic

### *B. Simulation Results*

Fig. 4.2: Read Cycle Simulation

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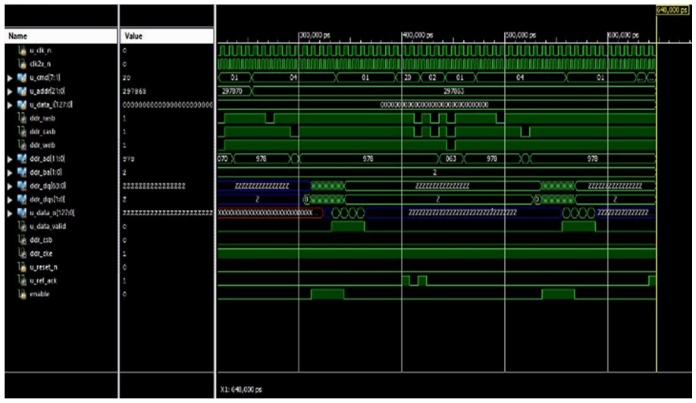

Fig. 4.3: Write Cycle Simulation

*C. Synthesis Report*

TABLE 4.1
Synthesis Report

| Component | Count |
|---|---|
| Speed | 256 Mbits/pin |
| Slices | 458 |
| Slice Flip Flops | 788 |
| 4 input LUTs | 319 |
| IOs | 378 |
| Bonded IOBs | 376 |
| GCLKs | 2 |

## V. CONCLUSIONS

Implementation of a 256Mb, 133MHz DDR SDRAM Data Controller architecture on FPGA is done that obviates high-speed, low-power data transmission between microprocessor (ALU) and memory devices. A digital FPGA path is introduced. A prototype implemented in Spartan-3E FPGA process operates at 256Mb and 133MHz with a 2.5V supply. The Language used is Verilog HDL. Xilinx (ISE) is used for the simulation and implementation purpose. This is operated in Base Mode Register.

## VI. ACKNOWLEDGMENT

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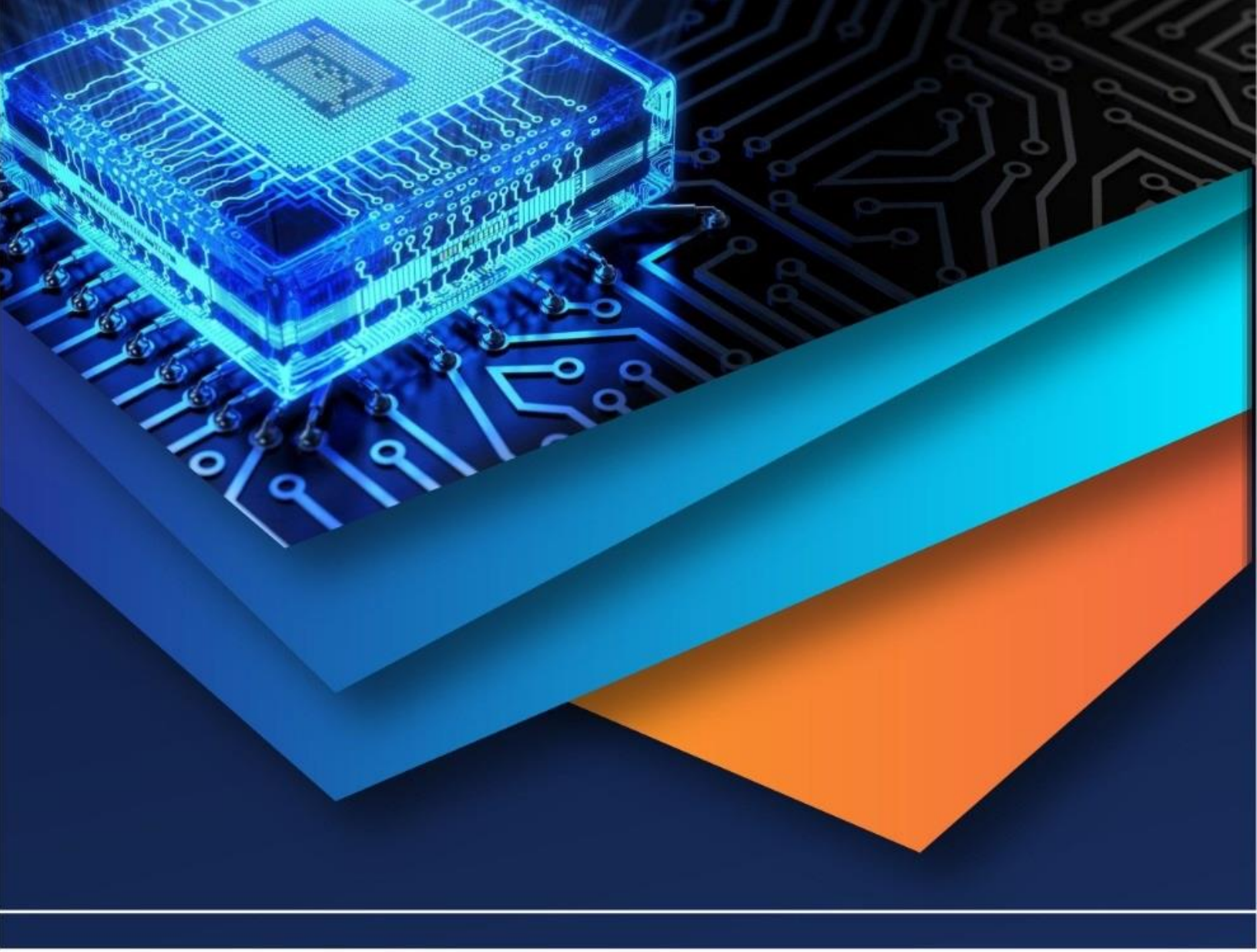

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