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Silicon Wafer Technologies: Past & Future

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Abstract: ***Silicon is now best substrate material for IC technologies. This paper is review about development of wafer technologies in past and future. Also discuss about silicon crystal growth, Silicon on Insulator technologies and CMOS devices capabilities. The roadmaps of industry manufacturing and future of silicon wafer technologies also discuss.***
Keywords*:* ***Silicon, Crystal Growth, Roadmap, CMOS, Wafer Technology.***

I. INTRODUCTION

Silicon is base material for Integrated circuit preparation. Silicon covers 90% of market of IC fabrication. It has several advantages than any other semiconductor like larger band gap, higher operating temperature, easily available and converted easily into SiO_2. The SiO_2 layer is effective insulator that helps to make stable structure of ICs. For application purpose, silicon is most adequate material, market also feeding more and more devices to silicon wafer. In 2010, silicon wafer production and sale was around $10 billion [1]. But some issues like active power dissipation, high leakage current etc. are limits the use of silicon, to overcome these problem replace the silicon with other materials. To increase higher band gap and breakdown voltage gallium nitride (GaN) grown on silicon surface, to increase operating frequency source/drain of MOSFET made by SiGe Cu used metallization.

In nature, Silicon is found as an oxide in the form of sand and Quartz. For fabrication process, Silicon must be in crystalline form i.e. very pure free from defects and uncontaminated. In general, 10^{22} atoms per cubic cm in silicon and therefore we require not more than one unwanted impurity on 10^9 silicon atoms[2]. This is a purity of one atom in a billion.

As we know that silicon as an element is not found in nature it is found as silicon dioxide in the form of quartz sand. There are several methods for obtaining pure silicon one of them is to first refine silicon dioxide with carbon in an arc furnace at very high temperature [3]. Which gives Si and Co_2. Than Co_2 evaporate as a gas and leaving behind impure silicon which is known as metallurgical grade silicon. Now next step to purify the silicon for that first we produce silicon tetra chloride by burning the silicon.

$$Si + 2Cl_2 \longrightarrow SiCl_4$$

$$SiCl_4 + H_2 \longrightarrow Si\,HCl_3 + HCl$$

Now this tri chloride is reduced by hydrogen to form very pure silicon which is known as Electrode grade silicon. EGS to produce a single crystals of silicon. It can be done by a method known as crystal growth.

II. SILICON SUBSTRATE MATERIALS TECHNOLOGY

An easy way to comply with IJRASET paper formatting requirements is to use this document as a template and simply type your text into it. In the 1950s, Crystal growth and substrate technologies are speedily evolving to become a specialty producing platform which will address the distinctive wants of the star business. Whereas elementary processes within the producing of element wafers are in situ, element producing technology has unendingly improved so as to satisfy the element wafer constant quantity capability and value necessary to sustain scaling progress on semiconductor and star business roadmaps [1]. Producing strategies ordinally employed in the business are made public in Fig. 1 and also the key aspects for varied processes are represented within the following sections. In the 1950, crystals were grownup principally by the float zone (FZ) method and wafers were engraved once diamond sprucing. However within the 1960, abundant of the elemental work for the present element business was initiated [2].

A. Production of Polysilicon

Metallurgical grade polysilicon is created through the reduction of oxide by mix it with carbon and heating, it usually in an electrical arc chamber, to over 1900 0C. Element created by this methodology usually contains 2% impurities though this might be reduced somewhat through the utilization of upper purity oxide and carbon feed materials. The foremost ordinarily used method for additional purification to electronic grade element converts the science grade material to trichlorosilane (TCS), that is in liquid kind and simply refined through succeeding distillation An alternative methodology of production involves decomposition of silane during a fluidized bed reactor (FBR) [4].

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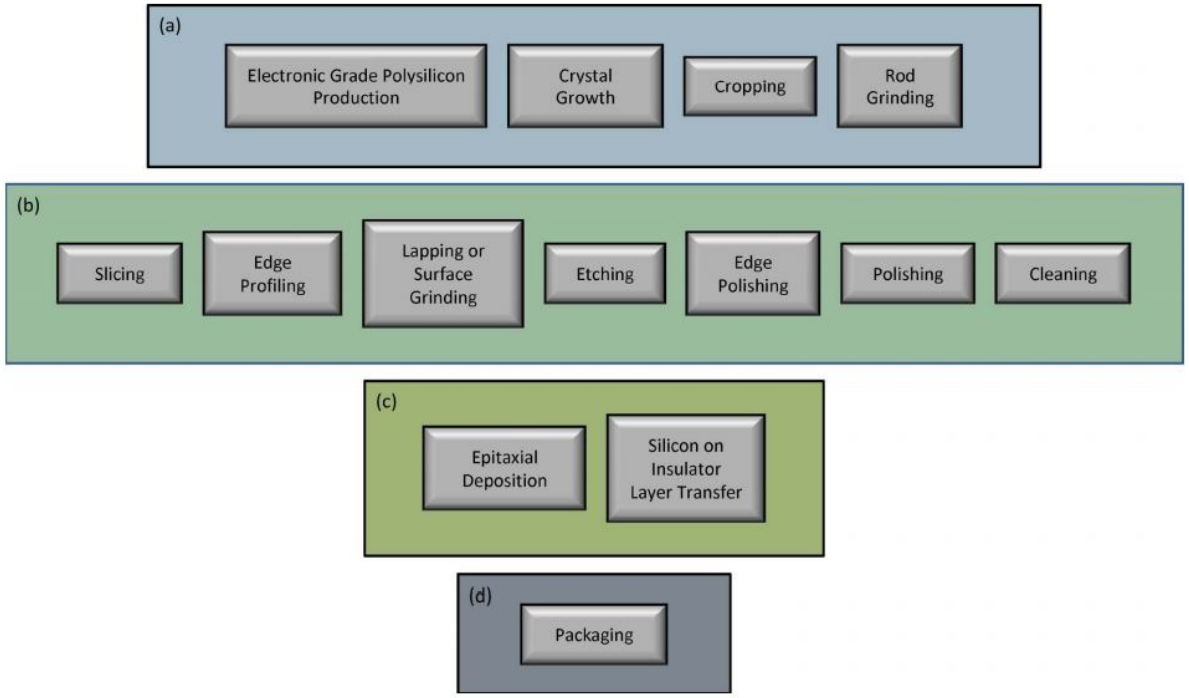

Fig 1: IC Development process (a) Silicon Development (b) Silicon Wafer Development (c) Layer Growth (d) Final Packaging

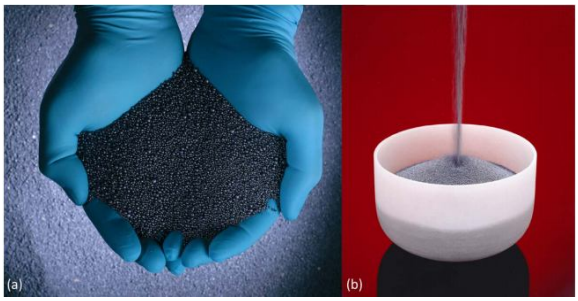

Fig. 2. Granular polysilicon

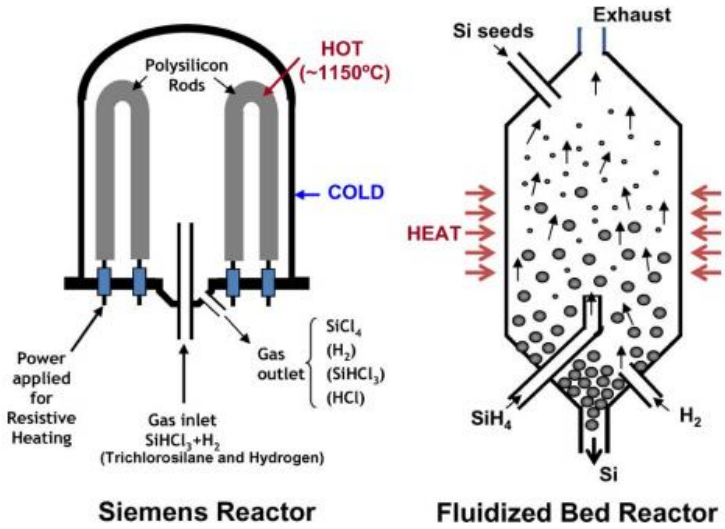

Fig. 3 Fluidized bed rectors (FBR)

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This technique utilizes heated silane and element gases, that are injected into very cheap of the reactor inflicting a bed of tiny element seed granules to become fluidized. The silane decomposes within the hot reactor and element is deposited on the seeds inflicting them to grow in size and weight. Once grownup to the specified size, the granules (Fig. 2) are extracted from very cheap of the reactor whereas recent seed particles are fed into the highest of the reactor. Fluidized bed reactors utilize nearly all the silane gas fed into the reactor, offer superior heat and mass transfer characteristics, and are energy economical [2]. As highlighted in Fig. 3, FBR method is additionally endless method whereas the Siemens method could be a batch method. Thus, the FBR method is a more economical than the Siemens method and is changing into a lot of wide adopted. Electronic grade polysilicon has impurities within the low elements per billion (ppb) vary or less, which is a necessary demand for production of semiconductor devices.

B. Growth of Single Crystal element

The business commonplace for production of monocrystalline element for semiconductors is that the Czochralski (CZ) methodology. Use of melt-based growth for semiconductor crystal growth was pioneered by Teal and small by demonstrating the expansion of single crystal Ge [3], [5]. Later, Teal and Buehler grew CZ–Si victimization constant technique, however they may solely grow injured single crystals of specific orientation [6]. The primary demonstration of dislocation-free CZ element crystal growth was incontestable in 1959 by Dash, employing a changed seeding technique [7] [8]. Growth of element crystals by the CZ methodology has been wide studied over the course of the subsequent 5 decades as shown in fig. 7. Dislocation-free, high-purity element crystals up to 450 metric linear unit in diameter are currently potential on a poster scale.

A great deal of effort was exhausted on distinguishing, characterizing, and reducing impurities within the CZ growth method, notably carbon, oxygen, and boron, that were at a lot of higher levels than those of FZ Si, and caused issues in sure device applications. With diligent effort and therefore the advent of low polysilicon from the Siemens method, the impurity levels of CZ were greatly reduced, and therefore the CZ method displaced the FZ method all told however a couple of specialty applications.

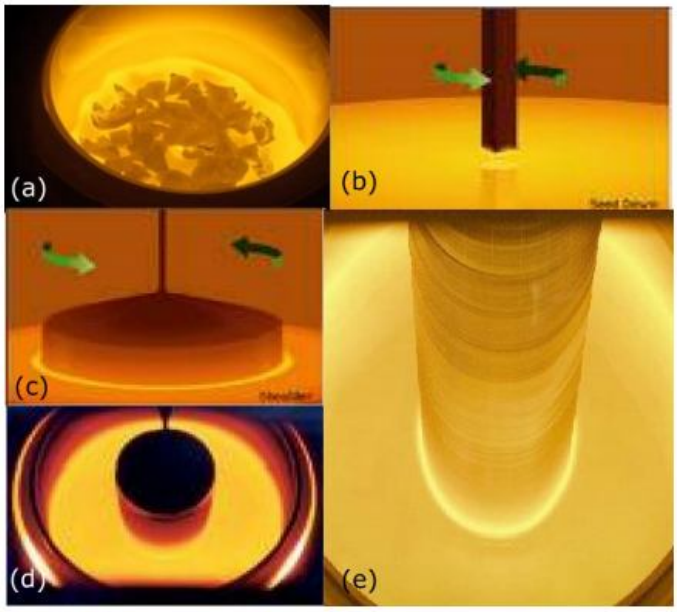

Fig 4. Czochralski crystal growth (a) meltdown; (b) seed dip; (c) top; (d) shoulder; and (e) body

C. Crystal Cropping and Grinding

Once the crystal has cooled, it's reserved from the crystal puller for machining. In observe, diameter management tolerances of the crystal actuation stage are of the order of millimetres, that is massive compared to the specified diameter tolerance of finished substrates [2]. Therefore, crystals are usually full-grown a couple of millimetres oversized on diameter and ground right down to the specified size before slicing. At first the shoulder and tail parts are removed with a diamond blade cropping saw and recycled. The body of the crystal is then sawed into lengths which will be accommodated by the next slicing operation, and ready for grinding to the specified diameter [9]. Within the days of smaller wafers a flat was ground on one facet to point crystallographic direction as determined by diffraction. However later, on larger wafers and within the interests of protective expanse for merchantable devices,

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the flat was replaced by a notch. D. Slicing the wafer production method (Fig. 5) starts with slicing of the crystal metal bar. Second styles of slicing ways are employed in the Si wafer industry i.e. the inner diameter (ID) saw and the wire saw. The ID saw uses a skinny ring-shaped blade with a diamond guaranteed region on the within fringe of the annulus. ID saws cut only 1 wafer at a time, taking a couple of minutes to slice every wafer from the crystal. Blade flexure throughout slicing light-emitting diode to warp and bow within the ensuing wafers and blade wear or poor blade dressing resulted in higher total thickness variation (TTV) from the saw. High TTV from the saw should be corrected by the downstream processes. Law makers worked on the matter of developing tensioning systems to regulate flexing of the ever agent blades needed to scale back kerf losses. A wire saw on the opposite hand takes many hours to chop through a crystal metal bar, however makes many hundred parallel saw cuts at the same time, wafering the complete metal bar in one operation. At crystal diameters larger than one hundred fifty millimetre, wire saws have established to be a lot of economical than ID saws with higher output and therefore the potential for lower kerf losses by exploitation agent wires.
Machining processes that turn out sleek flat polished surfaces usually have low throughputs and thus are dearer for a given capability demand as a result of a lot of machines are needed that successively needs more room on the mill floor, a lot of maintenance, and doubtless a lot of operators [10]. High output machines on the opposite hand cannot reach the surface quality needed for semiconductor wafers. As a result, a mix of machining processes is employed within which the initial processes are quick, rough cuts and ulterior steps use slower cuts to get rid of the harm from previous steps while not causation new harm. The fundamental sequence of steps is shown in Fig. 1(b) beginning with edge identification that applies a formed wheel to make a rounded wafer edge profile that is a lot of immune to breaking.

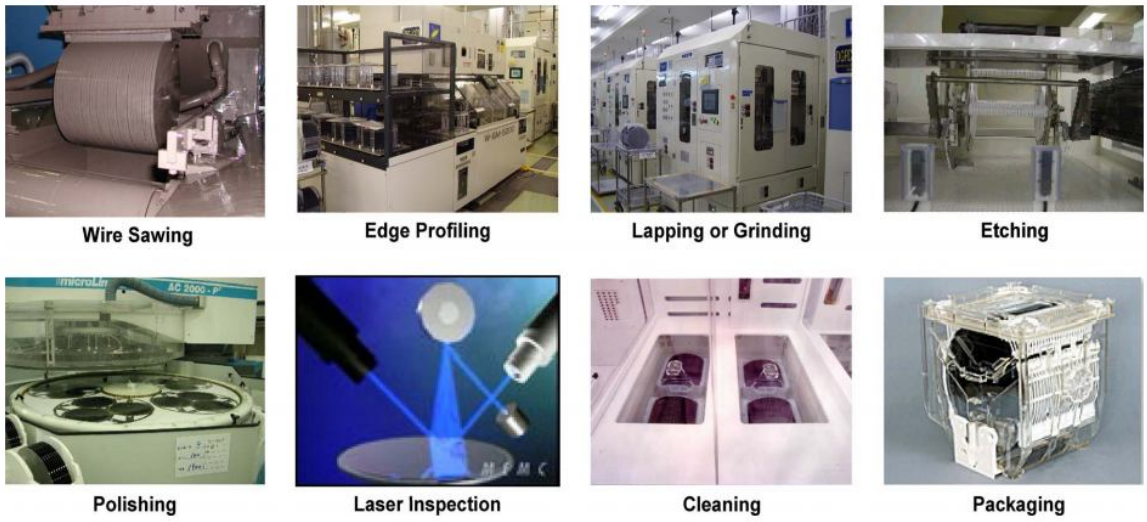

Figure 5. Sequential process of Silicon wafers manufacturing.

D. Lapping and Etching

As-cut wafers from a saw usually have a better TTV than that needed for progressive planography processes employed by device makers. This state is corrected by subjecting the wafers to a grinding (fixed abrasive) or covering (loose abrasive) method. The macroscopic flatness of wafers is often determined by this covering or grinding method [11]. Succeeding chemical etching removes the crystallographic injury that these processes manufacture however care should be taken that this etching not degrade the flatness. This is often achieved through selection of the etching chemistry, careful style and operation of the etching tanks, and therefore the fluid mechanics of the etchant flow. Etchants embrace caustic etches like KOH, that leave a comparatively rough surface however maintain a really high degree of macroscopic flatness or acid print, which may be optimized to provide a sander surface however far more seriously degrades the macroscopic flatness particularly close to the wafer edge [12]. The active elements of acid etching square measure hydrofluoric and azotic acids in either carboxylic acid or oxyacid, that square measure accustomed tailor the viciousness. If utilized in the proper manner and in appropriate tanks, acid etching will manufacture a sleek, shiny surface.

E. Polishing

In the ancient, single-side sharpening method, wafers were mounted on a flat sharpening plate with wax and therefore the exposed

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surface was ironed onto a rotating polymer pad soaked within the oxide suspension [11]. Developments over 5 decades embrace reduction in particulate contamination, which may cause scratches, coming up with sharpening machines with higher stability, understanding and rising pad wear mechanisms and pad dressing procedures yet as optimizing pressures, temperatures, and flow rates to optimize flatness. Suspension chemistry has additionally been improved with varied additives to extend removal rates and increase chemical purity to avoid undesirable metals like copper.

F. Cleaning

A clean chemical element surface is important to device performance. Contaminants will cause discharge, low breakdown voltage, no uniform compound growth, lithography errors, and plenty of different issues for device makers [11] [12].

The key phases in improvement a chemical element surface are:

1) Removal of insoluble organic contaminants with a 5: 1:1 binary compound: H_2O_2: NH_4OH solution
2) Stripping of a skinny oxide layer employing a diluted 50:1 H_2O: HF solution
3) Removal of ionic and serious metal contaminants employing a answer of 6:1:1 binary compound: H_2O_2 : HCl
4) Passivation of the extremely reactive blank, clean, chemical element surface in binary compound.

G. Epitaxy

During the primary 20 years of the semiconductor trade, most devices were designed on polished chemical element substrates, however as device densities inflated and CMOS architectures were adopted, epitaxial substrates became the popular selection among advanced logic and microchip makers [12]. At above >1000 ^{0}C temperature epitaxial layer was growth from chlorosilanes with vary high rate (2-4m/min) of deposition. This process control by transporting of gaseous phase precursors to surface. Epitaxy also performed at low 600 ^{0}C temperature from trichlorosilane to dichlorosilane to silane, growth rate also slow and this process also controlled through gaseous phase transport phenomenon.

III. ADVANCED SUBSTRATE TECHNOLOGIES

Technical challenges square measure several for each device and substrate suppliers, and as completely different solutions evolve, we have a tendency to see a divergence in device architectures and therefore the substrates upon that they're designed[1] [10]. Important challenges square measure highlighted within the 2010 Technology Roadmap for Semiconductors (ITRS) (see Table 1).

Table 1 International Technology Roadmap for Semiconductors

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*
DRAM ½ Pitch (nm) (contacted)	36	32	28	25	23	20	18
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	38	32	27	24	21	19	17
MPU Physical Gate Length (nm)	24	22	20	18	17	15	14
DRAM Total Chip Area (mm²)	56	44	23	37	29	23	19
DRAM Active Transistor Area (mm²)	17.8	14.1	10.4	16.4	13.0	10.4	8.2
MPU High-Performance Total Chip Area (mm²)	260	184	260	206	164	260	206
MPU High-Performance Active Transistor Area (mm²)	37.2	27.3	40.2	32.3	25.9	41.7	33.5
General Characteristics * (99% Chip Yield)							
Maximum Substrate Diameter (mm)—High-volume	300	300	300	450	450	450	450
Edge exclusion (mm)	2	2	2	2	2	2	2
Front surface particle size (nm), latex sphere equivalent (A)	≥45	≥45	≥32	≥32	≥32	≥22	≥22
Particles (cm^{-2}) ***	≤ 0.19	≤ 0.19	≤ 0.19	≤ 0.19	≤ 0.19	≤ 0.18	≤ 0.18
Particles (#/wf)****	≤ 134	≤ 132	≤ 131	≤ 294	≤ 291	≤ 288	≤ 285
Site flatness (nm), SFQR 26mm x 8 mm Site Size	≤36	≤32	≤28	≤25	≤23	≤20	≤18
Nanotopography, p-v, 2 mm dia. analysis area (I)	≤9	≤8	≤7	≤6	≤6	≤5	≤4
Epitaxial Wafer * (99% Chip Yield)							
Large structural epi defects (DRAM) (cm^{-2}) (B)***	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018
Large structural epi defects (MPU) (cm^{-2}) (B)***	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004
Small structural epi defects (DRAM) (cm^{-2}) (C)***	≤ 0.036	≤ 0.036	≤ 0.036	≤ 0.036	≤ 0.036	≤ 0.036	≤ 0.036
Small structural epi defects (MPU) (cm^{-2}) (C)***	≤ 0.008	≤ 0.008	≤ 0.008	≤ 0.008	≤ 0.008	≤ 0.008	≤ 0.008
Silicon-On-Insulator Wafer* (99% Chip Yield)							
Edge exclusion (mm)*****	2	2	2	2	2	2	2
Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (nm) (D)	46-71	43-65	40-60	38-56	35-52	33-48	31-45
Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3σ) (nm) (E)	17-22	17-21	16-20	15-18	14-17	14-17	14-16
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3σ) (nm) (F)	36-60	34-56	30-50	28-46	26-42	24-38	22-36
D_{LASOI} Large area SOI wafer defects (DRAM) (cm^{-2}) (G)***	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018	≤ 0.018
D_{LASOI} Large area SOI wafer defects (MPU) (cm^{-2}) (G)***	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004	≤ 0.004
D_{SASOI} Small area SOI wafer defects (DRAM) (cm^{-2}) (H)***	≤ 0.282	≤ 0.282	≤ 0.282	≤ 0.282	≤ 0.282	≤ 0.282	≤ 0.282
D_{SASOI} Small area SOI wafer defects (MPU) (cm^{-2}) (H)***	≤ 0.159	≤ 0.156	≤ 0.153	≤ 0.151	≤ 0.148	≤ 0.145	≤ 0.143

A. 450-mm Substrates

Wafer diameter modification needs a coordinated effort of the whole offer chain, wafer makers, instrumentality makers, and device makers. Whereas from a technical purpose they don't seem to be any elementary barriers, engineering challenges are vital. For the wafer providers, massive crystal growers, crystal handling systems, thermal process instrumentality (epi, RTA, furnaces), new safety concerns, wafer handling instrumentality, and automation systems would require a major style effort on the far side simple scaling of earlier instrumentality generations. Uniformity of wafer parametric over a pair of the world can gift additional challenges for wafer and device makers and their instrumentality suppliers. To boot, the introduction of 450-mm wafers would require vital effort come to agreement at intervals the trade on a way to achieve economic viability of such substrates [13]. From the device makers' stand, the economic presumption has historically been that the world of the wafer can double whereas the price of the process instrumentality can increase by a lesser quantity (30%) at roughly constant wafer turnout (except for lithography, metrology, and particle implantation, that account for ever larger shares of the entire process), leading to a lower device value on larger diameter wafers. For the wafer provider and therefore the instrumentality provider, the state of affairs is way totally different. For the wafer supplier, it takes a far larger volume of silicon, processed at associate inherently abundant lower turnout, to form an equivalent extent of silicon at larger wafer diameters than at smaller wafer diameters. Hence, the price per unit space of larger beginning wafer will increase for strictly physical reasons, even within the absence of monumental development and capital retooling prices which will be needed. For the instrumentality provider, a diameter increase incurs monumental style and development prices that should be recouped over a smaller put in base of tools. The matter of assignation of prices, risks, and come back on investment through the availability chain during a property fashion has over-involved the introduction of 450 metric linear unit, currently slated for 2014. At the terribly least, careful engineering value models can have to be compelled to be developed that area unit understood and in agreement to by the whole offer chain.

B. Silicon-on-Insulator Substrates

So far SOI wafers have remained solely tiny low fraction of the entire silicon market, primarily as a result of the price is considerably more than that of associate epitaxial wafer. In areas like MEMS, high voltage, optical waveguides, ultralow power, radiation hardened, and RF devices, the distinctive blessings of SOI justify the worth differential [1]. As capabilities improve and prices come back down, we must always expect the SOI wafer share to extend in alternative market segments. With continued scaling on the far side twenty two nm, the matter of Vth variations thanks to random dopant fluctuations (RDFs) within the channel implants accustomed management short channel effects could become intolerable, significantly for stable static random access memory (SRAM) operation [1][3]. The utilization of totally depleted SOI (FDSOI) transistors with undoped channels offers a possible resolution. However, the edge voltage of transistors designed around FDSOI technology may be an operate of the highest silicon layer thickness and at the 10–20-nm layer thickness needed, a 1-nm thickness variation corresponds to a couple of 25-mV variation in Vth, that places tight constraints on layer thickness uniformity. Management at these levels means the thickness uniformity demand is approaching the dimensions of typical surface peak to depression roughness for layer transfer technology. FDSOI are often combined with a 10–20-nm buried compound (BOX) layer [ultrathin body and BOX (UTB) transistors] to enhance short channel effects and open up the chance of dynamic threshold voltage management by applying back gate bias [33].

C. Looking on the far side ancient CMOS

The nonplanar semiconductor device structures like FinFETs provide another resolution to the issues of RDFs and short channel effects [14], [15]. Nonplanar transistors provide many performance blessings over planate transistors, however at the price of serious process challenges related to abandoning ancient planate design. Multigate transistors provide superior static management relative to single gate architectures. Corporations area unit getting down to commercialize multigate transistors at the 22-nm technology node on bulk silicon wafers [16]. Their development is anticipated to alter extension of silicon CMOS scaling into the sub-10-nm vary [17]. However, the necessities for skinny silicon films and extremely slim fins impose vital technical challenges to management the size of the fins and control variability iatrogenic by downstream processes, each of which can cause variation in device performance that scale back the benefits gained from the FinFET. FinFETs also can be fictitious on SOI wafers, employing a less complicated method flow that offsets the upper value of the SOI beginning wafer[15][16]. CMOS scaling on the far side FDSOI and FinFETs can doubtless involve the combination of upper quality channel materials on silicon. Candidate materials embrace InGaAs for rising lepton quality and Ge or InSb for rising hole quality [15]. The comparative challenges of group action higher quality channel materials like III-V or Ge in planate FDSOI structures versus in 3D semiconductor device structures can additional complicate the selection of beginning wafer. At this stage, it's not possible to predict the technical evolution and it's terribly

doubtless that different device manufacturers can adopt different solutions, and these solutions can doubtless need a spread of bulk and SOI substrate styles.

D. Integration With Compound Semiconductors

In several areas, silicon is probably going to be the bottom substrate for a few new materials integration. We have a tendency to area unit already seeing efforts to exchange sapphire or carbide with silicon for III-nitride materials [18]. whereas the barriers area unit formidable, thanks to thermal and lattice mismatches, some corporations area unit manufacturing GaN/Si substrates, that area unit at first finding use within the high-voltage power device market [19]. Further, tries area unit being created to enhance defect density to form them applicable for advanced devices like high brightness light-emitting diodes (LEDs) and lasers. In the end, every device manufacturer can realize the optimum resolution for its individual product combine in terms of value and performance and it looks doubtless that the solutions can vary across a spread of architectures and several other substrates. On the opposite hand, it looks quite bound that silicon in one kind or another can stay the semiconductor of selection for a minimum of another decade or 2 with various materials solely gaining share in niche segments of the semiconductor materials market.

IV. CONCLUSION

The drive for the electronics trade over the last forty years has been the relentless increase in integration density enabled by dimensional scaling and matched with the semiconductor device performance edges related to reducing metal–oxide–semiconductor junction transistor (MOSFET) essential dimensions [20]–[21]. The whole trade offer chain from material suppliers to instrumentality makers to device manufacturers have shared a standard trade roadmap that has charted the course for continued shrinking and inflated semiconductor device performance and chip practicality.

A more modern vital trend in semiconductor devices is that the inflated level of heterogeneous integration of numerous device varieties that add system practicality. Examples area unit the combos of ancient digital functions like central process unit (CPU) with non-digital functions like analog/mixed signal/RF, high voltage, passives, and sensors [22]. The mixture of those functions has generally been complete at the package level, however multiple functions area unit more and more combined in system-on chip approaches on single die. The trend for increasing integration of numerous device varieties to extend practicality has been represented as More than More [22] [23]. Silicon wafer styles can naturally vary for such a various set of device varieties. Wafer needs are determined way more by the device operate than by dimensional scaling.

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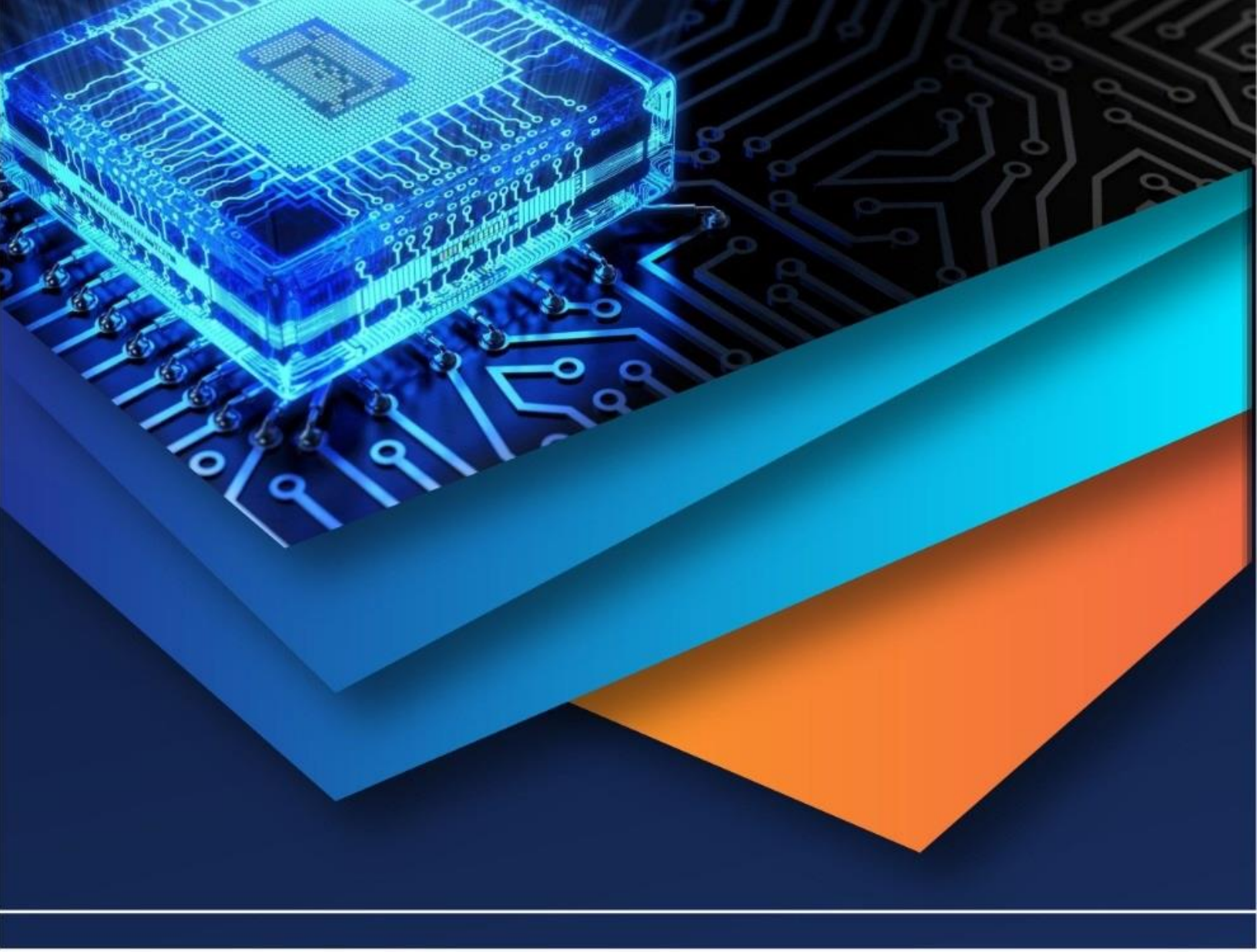

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