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The Modified SEPIC Converter with Extra Boost Unit and Without Coupling Inductor for PV Application

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Abstract-In this paper, the modified SEPIC converter with extra boost circuit and without coupling inductor is proposed for PV application using perturb and observe mppt algorithm. The proposed DC-DC converter has only one MOSFET switch with minimum voltage stress and this reduces the complex circuit design. The proposed converter is connected in between PV panel and load to obtain high voltage without extreme duty ratio. In this paper input voltage of 40V is obtained from PV panel is fed to converter in order to obtained output voltage of 400V with switching frequency of 100kHz. Thecircuit operation and passive parameter design of this proposed converter are discussed in details.
Keywords-SEPIC, MPPT algorithm,PV panel.

I. INTRODUCTION

Today, Indian energy scenario is mainly focuses on harvesting and maximum usage of green energy resources such as fuel cell, wind energy and solar energy etc, due to depleting nature of conventional fuels and increasing energy demand of society. In order to meet demand the high voltage DC –DC converters must be incorporate between PV panels and grid. As PV panel have less output voltage of about 12 to 40 V, these must be boost to 440 V for grid applications. Therefore, DC-DC converter having high voltage output required to be placed between PV array and high voltage dc grid.Unfortunately, conventional high voltage converter are not available because of high duty ratio and complex circuit design .In order to have high voltage converters, following type of converter have been proposed by 1) addition of switching capacitors or switching inductors to conventional converters[1-2]; 2) series connection of outputs [3-4];3) combining output of several conventional converters[5];4) integrating coupled inductor and voltage-doubling circuit or switching inductor[6-11]; 5) interleaving technique[12-13].however ,all of these techniques have their own demerits. High setup gain, simple modified control structure, higher efficiency and minimum voltage stress are the features still needed.

In this paper, the modified SEPIC converter with extra boost unit circuit and without inductor coupled is proposed forPV application using Perturbs and observe MPPT algorithm.It produces higher voltage ratio, reduced voltage stress of switch and continuous operation of input current.

II. PV CELL MODELING AND MPPT ALGORITHM

A. PV CELL MODELLING

The circuit configuration of PV cell is shown in fig.1.In this circuit R_s is series resistance of PN junction cell and R_{sh} is shunt resistance which is inversely in relation with leakage current to the ground. I_D and I_{sh} are diode current and shunt leakage current, where output current I is obtained by applying KCL.

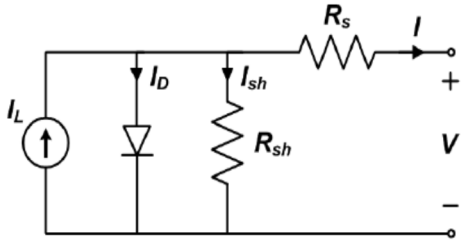

Fig .1. Circuit configuration of PV cell.

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$$I_L = I_{Ph} - (I_d + I_{sh}) \quad (1)$$

Above equation is simplified by taking $I_d + I_{sh} = I_o$ and hence equation becomes

$$I_L = I_{Ph} - I_O \quad (2)$$

Photon current is generated on absorption of solar radiation; hence photocurrent is directly proportional to variation of solar irradiance and temperature, is given by.

$$I_{ph} = (I_{scr} + k_i \Delta T)\frac{G}{G_r} \quad (3)$$

Where I_{scr} is short circuit current at normal conditions (25^0C and 1000w/m^2), k_i is short circuit current temperature coefficient. G is solar irradiance in W/m^2 and G_r is nominal irradiance in normal conditions (25^0C and 1000w/m^2).ΔT is difference ofoperating temperature and nominal operating temperature (T – T_{ref}).Reverse saturation current is given by.

$$I_d = I_{rs} * \left(\frac{T}{T_{ref}}\right)^3 exp\left[\left(\frac{qE_{qo}}{AK} * \frac{\Delta T}{T_{ref}T}\right)\right] \quad (4)$$

Where Irs is reverse saturation current for nominal temperature and irradiance and Ego is band gap energy of semiconductor material, current I is given by

$$I = I_L - I_O(\exp(q\frac{V+IR_S}{AKT})\text{-}1) - \frac{V+IR_S}{R_P} \quad (5)$$

B. Perturb and observe algorithm

This method is widely used, the operating output voltage is sampled and then it changes the operating output voltage in the required direction and samples the dP/dV. If $\frac{dp}{dv}$ is positive, then it increases the output voltage towards the MPP till $\frac{dp}{dv}$ is negative. This iteration is continues till the algorithm reaches the final MPP.This is not applicable when then solar irradiation various continuously. The voltage never reaches the required value, but perturbs in between the maximum power point (MPP).

III. OPEATION OF PROPOSED CONVERTER

The proposed converter circuit configuration is shown below in Fig.2,It is obtained from a conventional SEPIC converter ,where capacitance C_1, inductance L_1,diodes D_1 and D_2 ,forms an extra boost unit circuit, while capacitance C_3, and diode D_3 are forms an clamping circuit for MOSFET switch S .For the study of proposed converter ,let the following assumptions are made :1) converter is operated in steady state mode.2) all components are ideal;3) C2 andC3 are equal, Cout is more in order to make constant output voltage.

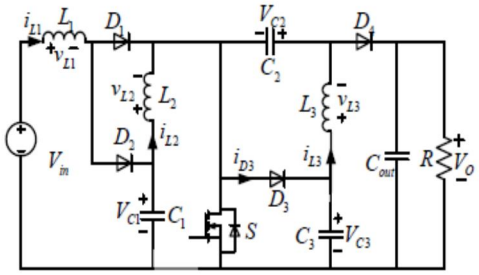

Fig.2.Single switch proposed converter.

Mode I [t_0-t_1]: When t=t_0, switch S is switch on. Diode D_1isforward biased, while diodes D_2, D_3 and D_4 are reverse biased. The circuit configuration and direction of current in this mode is shown in Fig. 3.Intitialy assumed that all capacitors are fully charged, in this mode, the input voltage V_{in}energizes the inductor L_1 viaD_1 and switch S. Then the inductor voltage V_{L1} across L_1 isV_{in}. The capacitor C_1 energizes inductor L_2via switch S, and then the inductor voltage V_{L2} across L_2 isV_{C1}. The capacitor C_3 energizes $L_3$and C_2

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viaswitch S, and then the inductor voltage V_{L3}across L_3 (V_{C3}-V_{C2}). So, the inductor currents i_{L1}, i_{L2} and i_{L3}linearlyincrease. The capacitor C_{out} gives stored energy to the load R, and makes the output voltage $V_o$constant. When t=t_1, Switch s is turned off, Mode I completed.

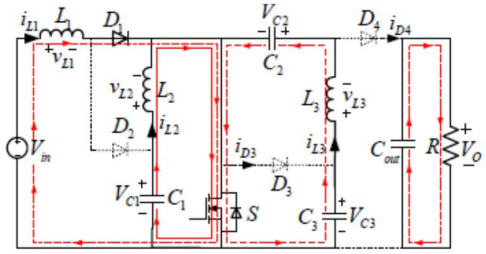

Fig .3.Circuit configuration of mode I in CCM.

Mode II [t_1-t_2]: When t=t_1, switch S is turned off. D_1 is reverse biased, while D_2, D_3 and D_4 are forward biased. The circuit configuration and direction of current in this mode is shown in Fig.5. Capacitor C_1 is charges by the input voltage $V_{in}$and inductor L_1 viaD$_2$ and V_{L1} is (V_{in}-V_{C1}). At the same time, V_{in}, L_1 and L_2charges C_3viaD$_2$, then V_{L2} is (V_{C1}-V_{C3}). Moreover, the stored energy of V_{in}, L_1, L_2 and L_3 supply to $C_{out}$and load R,and V_{L3} is equal to -V_{C2}.So, the inductor currents i_{L1}, $i_{L2}$and i_{L3} decrease linearly.When t=t_2, switch S is turned on and mode II is completed.

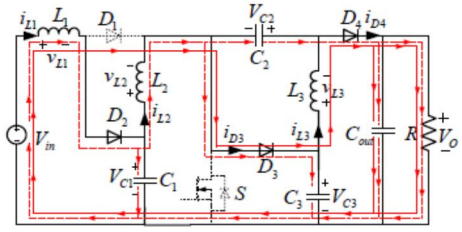

Fig .4.circuit configuration of mode IIin CCM.

From inductor voltage second balanced principle, we have

$$D\,V_{in} = (1-D)\,(V_{C1}-V_{In}) \quad (6)$$

$$DV_{C1} = (1-D)\,(V_{C3}-V_{C2}) \quad (7)$$

$$D\,(V_{C3}-V_{C2}) = (1-D)\,V_{C2} \quad (8)$$

Assuming capacitor voltage is constant during steady state operation from Equation (6), (7), (8), capacitor voltages are,

$$V_{in=}\,(1-D)V_{C1} \quad (9)$$

$$V_{C1} = (1-D)V_{C3} \quad (10)$$

$$V_{C2} = DV_{C3} \quad (11)$$

During stage II

$$V_O = V_{C2}+V_{C3} \quad (12)$$

Voltage gain in CCM mode is expressed by

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{(1+D)}{(1-D)^2} \quad (13)$$

IV. PASSIVE PARAMETER DESIGN

A. *Inductor design*

From fig.3.inductor L1 current ripple in CCM is expressed by

$$\Delta i_{L1} = \frac{V_{in}D}{f_S L_1} \quad (14)$$

$$L_1 = \frac{V_{in}D}{f_S \Delta i_{L1}} = \frac{V_{in}D}{\Delta i\% I_{L1} f_S} \quad (15)$$

Where $\nabla i\%$= inductor current ripple acceptance.

Similarly, inductor L_2 and L_3 are defined by

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$$L_2 = \frac{V_{C1}D}{f_S \Delta i_{L2}} = \frac{V_{C1}D}{\Delta i\% I_{L2} f_S} \quad (16)$$

$$L_3 = \frac{(V_{C3}-V_{C2})D}{f_S \Delta i_{L3}} = \frac{V_{C1}D}{\Delta i\% I_{L3} f_S} \quad (17)$$

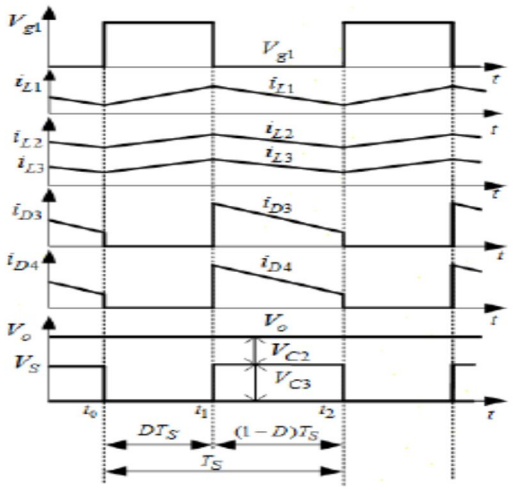

Fig.5.Theoretical wave form of CCM mode.

From Fig.4, the below current relationships are obtained, for mode I

$$i_{C3} = -i_{L2} \quad (18)$$

$$i_{C2} = -i_{C3} = i_{L3} \quad (19)$$

From mode II

$$i_{C1} = i_{L1} - i_{L2} \quad (20)$$

$$i_{C2} = -i_{C3} = i_{L3} - I_o \quad (21)$$

Fromcapacitor ampere second balance principle, we have

$$I_{L2} = (1\text{-}D)\, I_{L3} \quad (22)$$

$$I_{L3} = (1\text{-}D)\, I_O \quad (23)$$

If the power output Po, converter$efficiency\eta$ and resistive load R are known, as

$$I_{L1} = I_{in} = \frac{P_o}{\eta V_{in}} \quad (24)$$

$$I_O = \sqrt{\frac{P_O}{R}} \quad (25)$$

B. Capacitor design

Since capacitor C_2 current is equal to that of C_3 during mode I, the voltage potential of C_2 or C_3 is expressed by

$$\Delta V_{C2} = \frac{I_{L3}D}{C_2 f_s} \quad (26)$$

$$\Delta V_{C3} = \frac{I_{L3}D}{C_3 f_s} \quad (27)$$

Then

$$C_2 = C_3 = \frac{I_{L3}D}{\Delta V\% V_{C3} f_s} \quad (28)$$

Where, ΔV% = capacitor voltage ripple acceptance, in addition, the capacitorC_1 and $C_{out}$are large in order to keep the constant output voltage.

C . Semiconductor components design

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From Fig.3 and Fig.4,V_{DS} of the switch S in mode II is V_{C3}, the diode voltage of D_1 is V_{L2} in mode II or V_{C3} - V_{C1}, that diode voltage on D_2 equals to V_{L2} or V_{C1} in mode I, diode voltage of D_3 isV_{C3}, and diode voltageD_4 equals to the difference between Vo and V_{C2}. Then we have

$$V_{DS}=V_{C3}=\frac{V_{in}}{(1-D)^2}=\frac{V_O}{1+D} \quad (29)$$

$$V_{D1}=V_{C3}-V_{C1}=\frac{D}{(1-D)^2}V_{in}=\frac{D}{1+D}V_o \quad (30)$$

$$V_{D2}=V_{L2}=V_{C1}=\frac{V_{in}}{1-D}=\frac{(1-D)}{(1+D)}V_O \quad (31)$$

$$V_{D3}=V_{C3}=\frac{D}{1+D}V_o \quad (32)$$

$$V_{D4}=V_o-V_{C2}=\frac{D}{1+D}V_o \quad (33)$$

Since current via switch *S* in mode I is the summation of inductor currents i_{L1}, i_{L2} and i_{L3}, then peakcurrent in the switch will be

$$I_{SMAX}=\left(\frac{1+\Delta i\%}{2}\right)(I_{L1}+I_{L2}+I_{L3}) \quad (34)$$

Both diode currentsi_{D1} and i_{D2} are part of inductor currenti_{L1}, and then the peak diode currents of i_{D1} and i_{D2} will be

$$I_{D1MAX}=I_{D2MAX}=\left(\frac{1+\Delta i\%}{2}\right)I_{L1} \quad (35)$$

It is known that $i_{D3}=i_{L2}+i_{C2}=i_{L3}+i_{C3}$,$i_{C2}=i_{C3}$in mode II,then peak current of diodei_{D3} is

$$I_{D3MAX}=\left(\frac{4+2\Delta i\%}{8}\right)(I_{L2}+I_{L3}) \quad (36)$$

Finally, the current via D_4 is output current I_o

V. RESULTS AND DISCUSSION

In order to analyised the theoretical analysis, the operation of proposed Converter is simulated using MATLAB simulink and shown below Fig.6 and component design values are listed in table 1

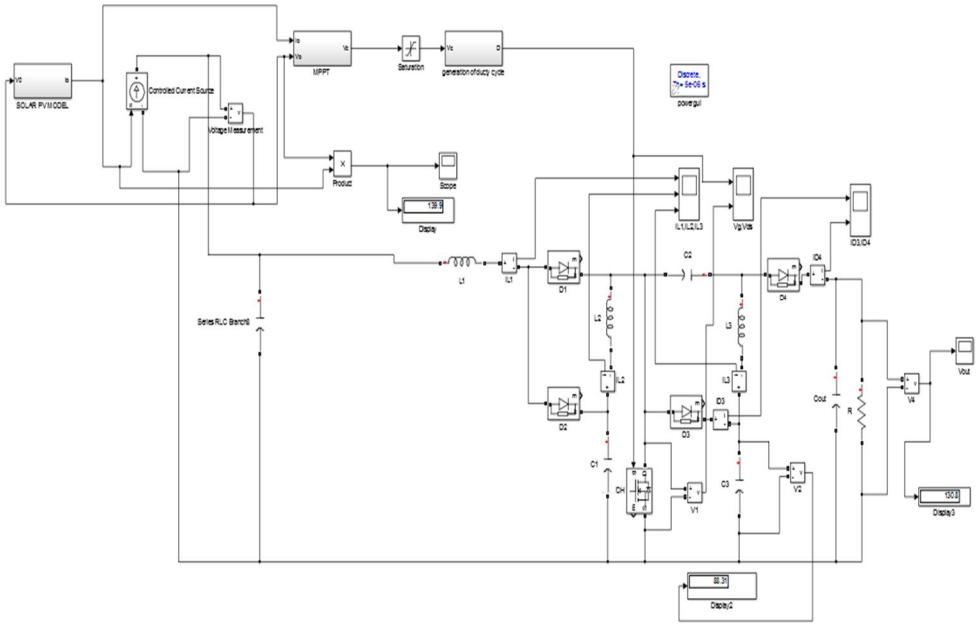

Fig.6.MATLAB/simulink model for proposed converter.

The simulation waveforms of inductor currents I_{L1},I_{L2} and I_{L3}, wave form of switching pulse generation and voltage across switch S and output voltage waveform are shown in Fig.7, Fig.8, and Fig.9 respectively. Obviously, the inductors current are continuous. So the converter is operating in CCM. From all the above, the simulation results agree with the theoretical analysis.

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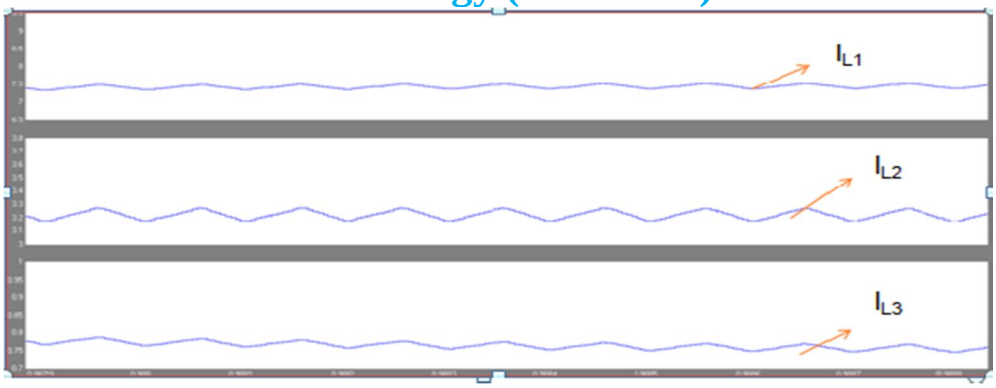

Fig.7.Inductor current waveforms.

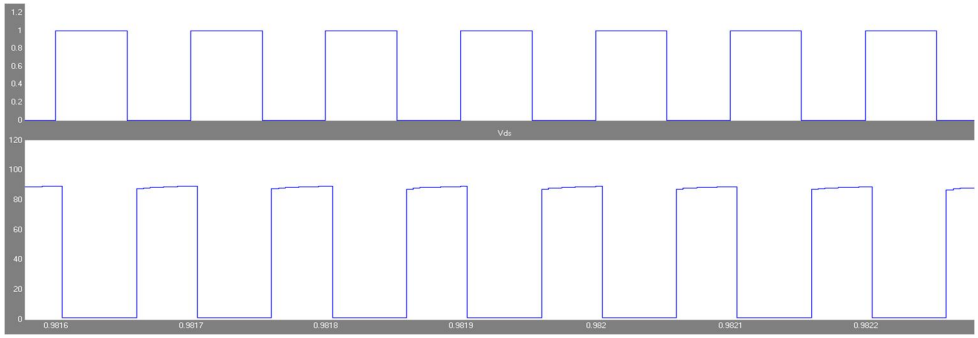

Fig.8. pulse generation and voltage waveform of switch S.

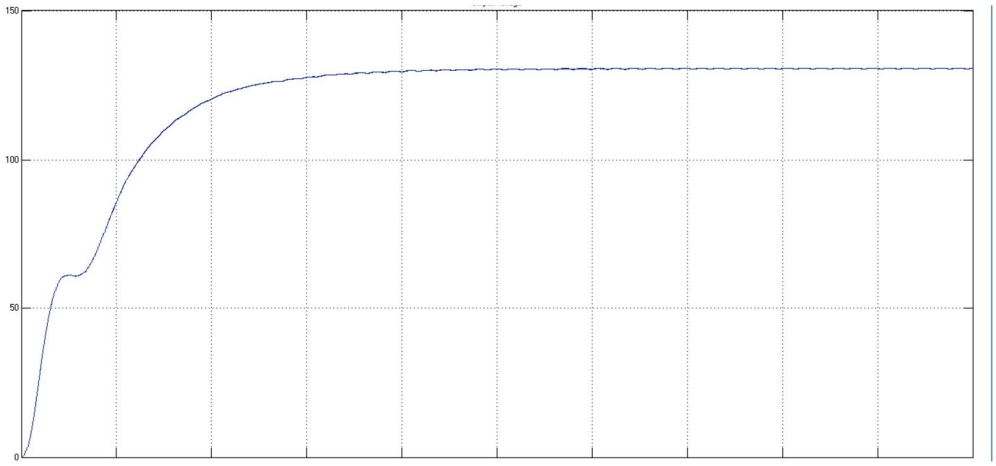
Fig.9.Output voltage waveform.

VI. CONCLUTION

In this paper,the modified SEPIC converter with extra boost unit circuit and without coupling inductor is proposed. It produces high voltage output without coupling inductor.Moreover, there is one MOSFET switch and the peak voltages of semiconductor switch are less than the output voltage, this makes the power switch with lower rating and all these features made this proposed converter suitable for PV application.

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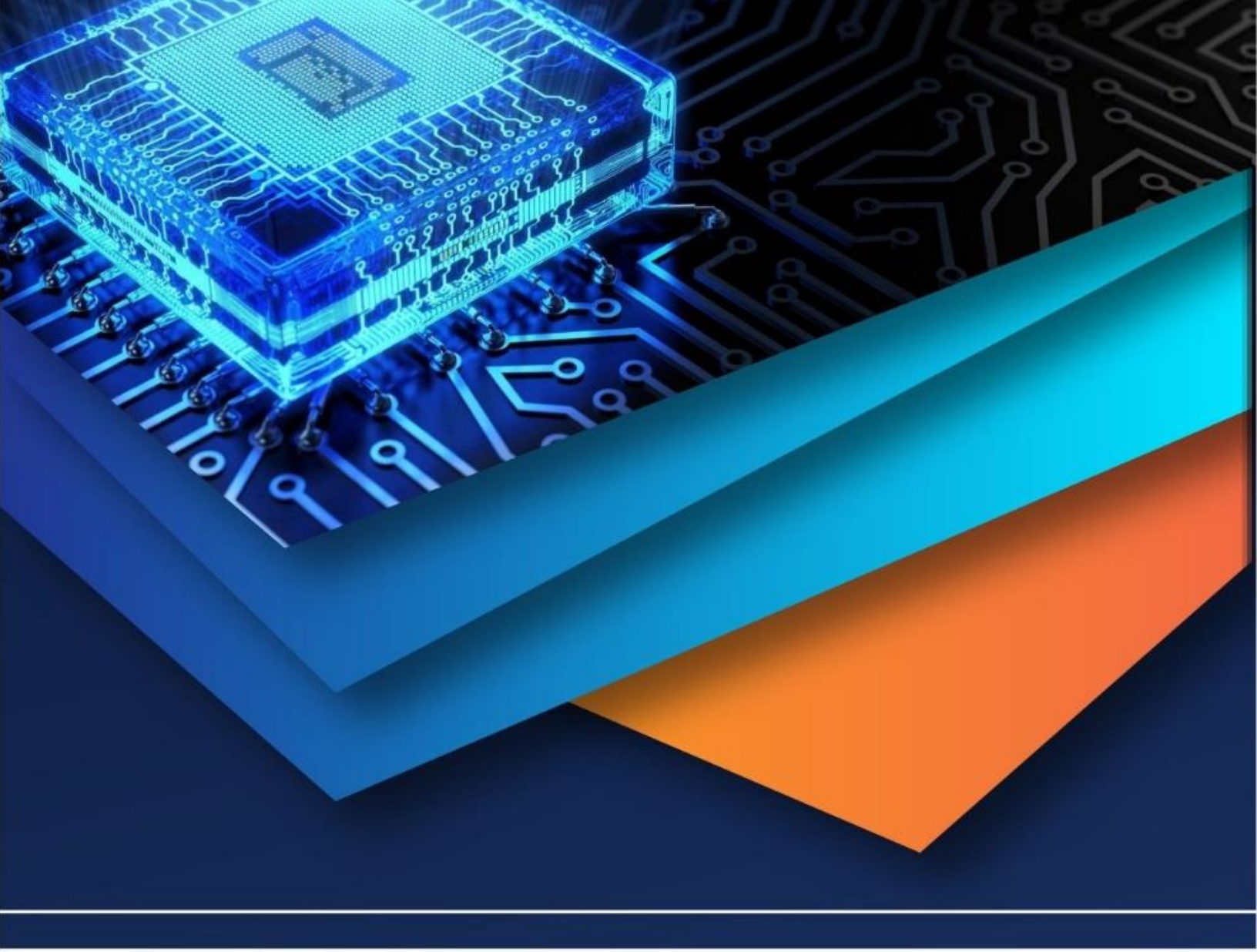

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