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Performance Improvement of Asymmetrical Multilevel Inverter with Different Optimization Algorithms

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Abstract: ***This paper presents a new asymmetrical multilevel inverter with Improved Performance by using different Optimization Algorithms. Each module produces 13 levels with four unequal DC sources and 10 switches. The proposed module makes some preferable features with a better quality than similar modules such as the low number of semiconductors and DC sources and low switching frequency. Also, this module is able to create a negative level without any additional circuit such as an H-bridge which results in reduction of voltage stress on switches. Cascade connection of the proposed structure leads to a modular topology with more levels and higher voltages. Selective harmonics elimination pulse width modulation (SHE-PWM) scheme is used to achieve high quality output voltage with lower harmonics. In this paper Particle Swarm Optimization (PSO) and Differential Evolution (DE) methods are used to generate the Pulse widths for selected Harmonic Elimination. MATLAB simulation results are presented to validate the proposed module performance. Module output voltage satisfies harmonics standard (IEEE519) without any filter in output.***

Index Terms—Asymmetric, components, module, multilevelinverter, power electronics, selective harmonics elimination, Particle Swarm Optimization& Differential Evaluation.

I. INTRODUCTION

Multilevel inverters (MLIs) have been innovated as necessary cost benefit devices with a wide range of applications. They have been in the focus for decades because of interesting features such as high quality output voltage, operation in high voltage/power, low stress on switches, etc. Multilevel converters have a wide range of applications which has rapidly developed the area of power electronics with good potential for further technology [1-6]. They canbe used in photovoltaic systems, wind farms, and HVDC systems. Multilevel converters are different arrangements of semiconductor switches with DC links to create N-level output waveform which are divided into three main categories [7]: Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascade H-Bridge (CHB). In 1981, NPC was introduced as the first multilevel converter which can be used in medium voltage applications [8]. Early 1990s, FC was presented [9] and in 1996, CHB was reintroduced [10]. Design of multilevel inverters depends on the number of voltage levels, number of semiconductor devices, output quality, number of DC supplies and DC link capacitors, THD amplitude, maximum voltage level, creating positive and negative level, modularity, switch stress and total standing voltage (TSV).

Researchers presented different types of modular multilevel inverters. As shown in Fig.1.a, each level is created by two switches and one source in [11]. These levels are connected in series together to achieve positive voltage levels and an auxiliary H-bridge circuit is used to create alternative voltage. Note that, H-bridge switches tolerate more voltages than other switches. As shown in Fig.1.b, the stress of H-bridge switches is divided between each sub-module [12]. Two capacitors are added for each DC source to reach more voltage levels with the penalty of using more components. Researchers tried to reach more levels with lower components. Asymmetric multilevel inverters which have unequal DC links become interesting in order to increase the quality of output waveform by minimizing the number of components. Modules are designed based on optimal using of DC links by reduced switches [13-15]. Other MLI topologies are proposed in [16-17] which are shown in Fig.1.f & Fig.1.g Also some interesting MLI topologies are investigated in [18-19].

One of the important factors of MLI design for high voltage applications is high voltage stress on the switches of the output H-bridge. Therefore, a redesign is vital to reduce the stress of the switches by dividing H-bridge voltage into all sub-modules in order to have a uniform stress on all switches which in turn leads to the increasing number of semiconductors and total standing voltage (TSV) of the module. This paper aims to achieve maximum capacity from DC link by a suitable arrangement of switches which improves economic implementation cost, switching frequency, TSV, number of levels, and THD. It presents a new asymmetric mul-

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tilevel module based on cascade category which does not need any additional circuit to create negative voltage levels. Also, it makes 13 levels by reduced switches. Section II illustrates proposed multilevel inverters including Module description, switching patterns, cascade connection and comparison table with similar modules. Selective harmonic elimination (SHE) is introduced for switching modulation in section 3. Simulation circuit is presented in Section 4. Experimental results and comparison different method for Pulse width generation are shown in sections 5. Conclusions are presented in section 6.

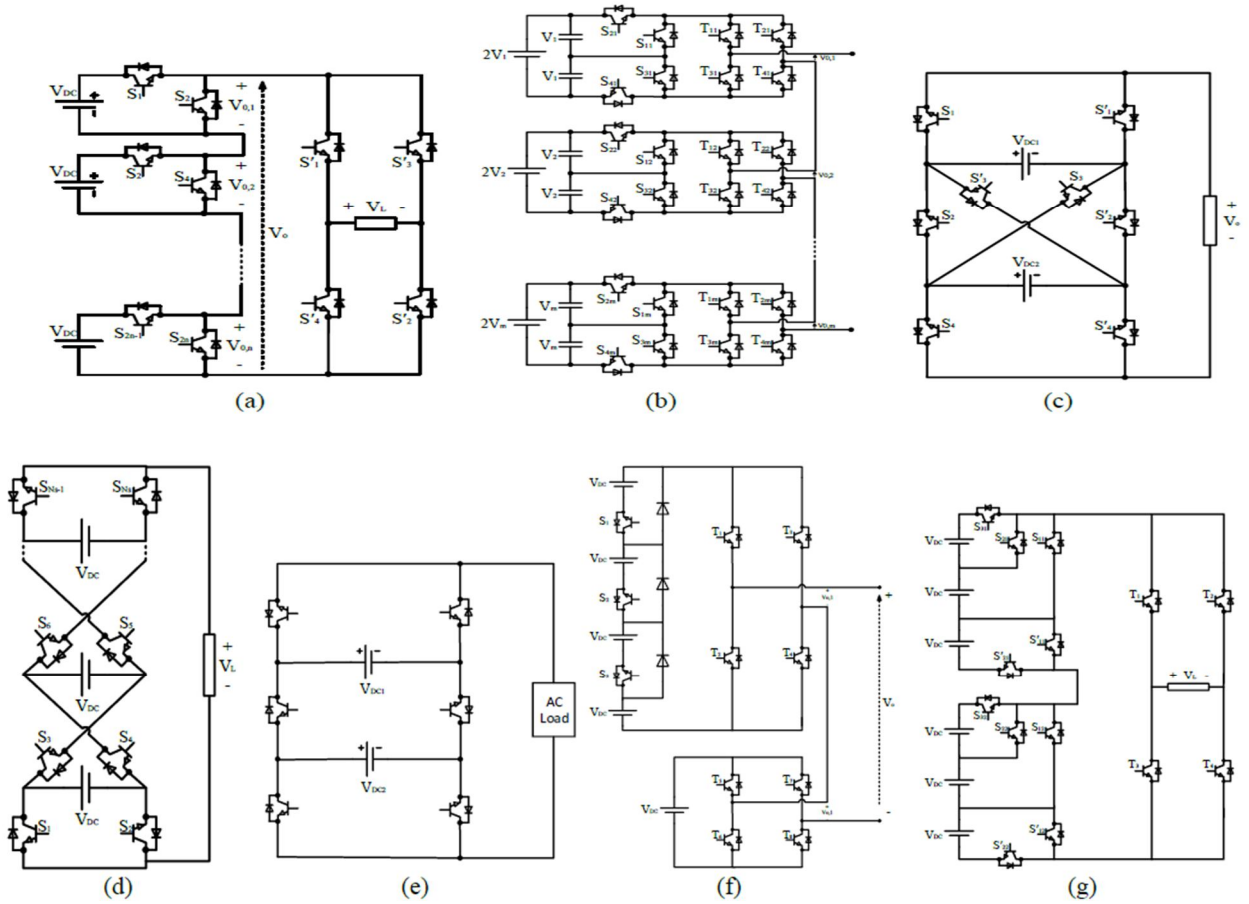

Fig.1 some modular multilevel inverter topologies

II. PROPOSED MOUDLE

Fig.2 shows a general schematic diagram of a typical asymmetrical multilevel inverter with two DC links for description of multilevel operation. Unequal DC links can be arranged with different connections (through switching components) in order to achieve high number of voltage levels.

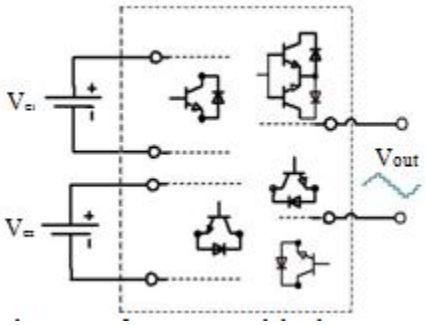

Fig.2 The general structure of asymmetric multilevel inverters

For example, assuming V_{C1}=V_{DC}andV_{C2}=2V_{DC}, voltage levels of ± V_{DC} ،±2V_{DC} and ±3V_{DC} can be achieved by choosing suitable paths

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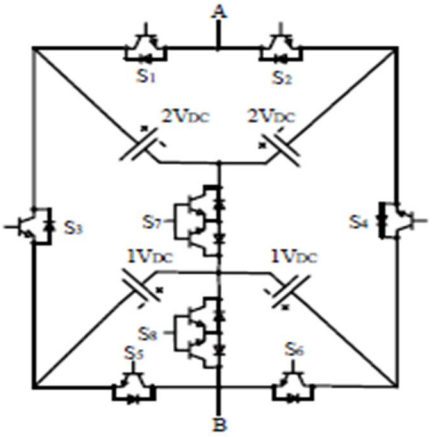
from switches and DC links depends on the module topology. Using this idea for multilevel inverters, a different ratio of DC link voltages may be

utilized to generate the different number of output voltage levels.Elimination in harmonic content peak with a same switching frequency and the same structure is approximately expected by increasing the number of output voltage levels in the asymmetrical inverter [20].

A. Module Configuration

This paper introduces a new topology of Improved asymmetric multilevel modular with a new component arrangement including 10 switches, 10 diodes and 4 unequal DC sources (two $2V_{DC}$, two$1V_{DC}$) named as modular/Envelope type (E-Type). This arrangement synthesizes voltage sources produces 13 levels (6 positive levels, 6 negative levels and zero level) without any additional circuit. The main concept of this circuit is to create different paths from different sides of a DC source to be connected to other sources. Fig.3 shows the configuration of asymmetrical module in which DC sources are located in the middle of the circuit and are connected together to form different voltage levels via surrounding switch (S1-S6). A bidirectional switch (S7) is required to avoid short circuit of DC sources on left or right sides of the module. Another bidirectional switch (S8) is also needed to achieve voltage levels of $\pm 5V_{DC}$. Different switching conditions of this structure are shown in Fig.3 and Table I.



(a)

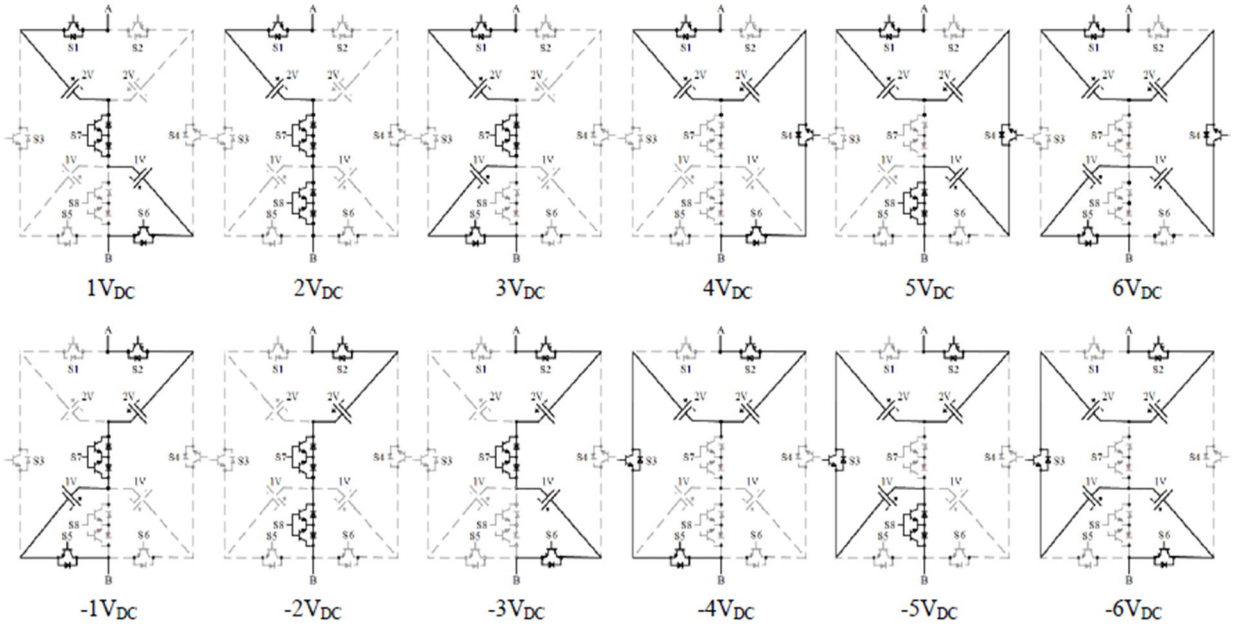


Fig. 3 Proposed E-Type module of multilevel inverter (a) Circuit topology (b)different switching states

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TABLE I
SWITCHING TABLE

		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Positive Level	$1V_{DC}$	1	0	0	0	0	1	1	0
	$2V_{DC}$	1	0	0	0	0	0	1	1
	$3V_{DC}$	1	0	0	0	1	0	1	0
	$4V_{DC}$	1	0	0	1	0	1	0	0
	$5V_{DC}$	1	0	0	1	0	0	0	1
	$6V_{DC}$	1	0	0	1	1	0	0	0
Negative level	$-1V_{DC}$	0	1	0	0	1	0	1	0
	$-2V_{DC}$	0	1	0	0	0	0	1	1
	$-3V_{DC}$	0	1	0	0	0	1	1	0
	$-4V_{DC}$	0	1	1	0	1	0	0	0
	$-5V_{DC}$	0	1	1	0	0	0	0	1
	$-6V_{DC}$	0	1	1	0	0	1	0	0

As shown in Table I, switch pairs (S1, S4) and (S2, S3) belong to positive and negative levels, respectively. In addition, (S1, S2) and (S3, S4) cannot be on at the same time. Fig.4 shows output voltage of the proposed inverter with the associated pulse pattern in one cycle of fundamental voltage. As shown in Fig.4, switches S1, S2, S3, S4 and S7 are turned on and off in low frequency which reduces switching losses to a great extent. Other switches also operate in a reasonable switching frequency. Table II shows comparison of different modular type multilevel inverters.

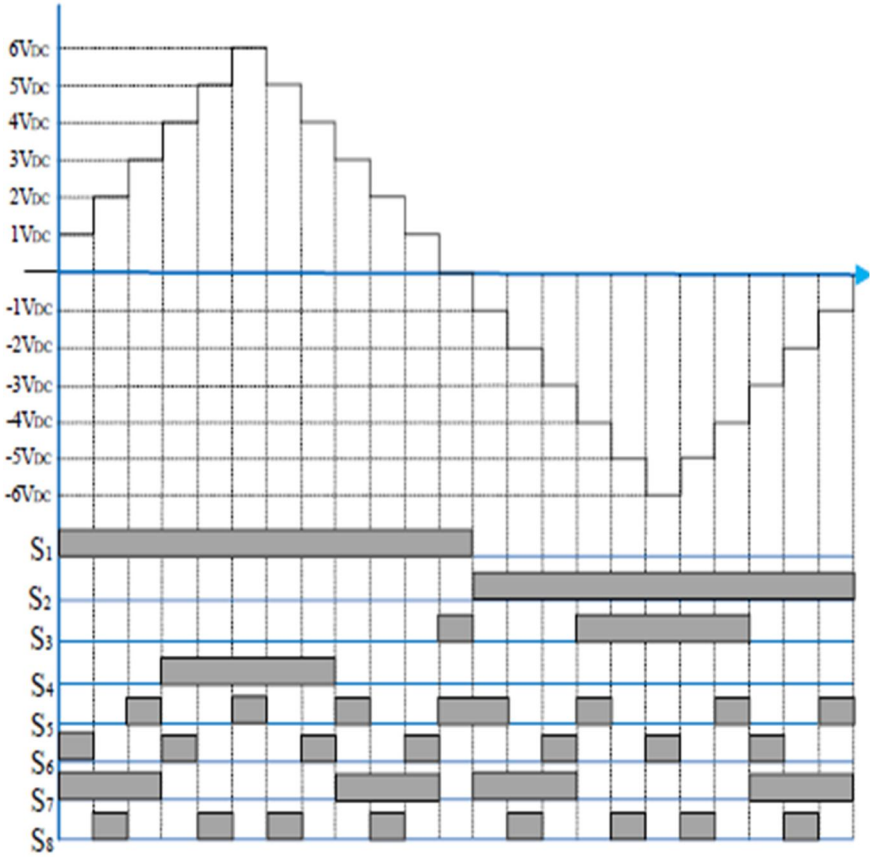

Fig.4 switching pattern of proposed converter in one cycle

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TABLE II

COMPARISON OF SOME MODULAR MULTILEVEL INVERTER TOPOLOGY

	NPC	FC	CHB	MLDCL [11]	2CLHB [12]	CSMLI [14]	U-cell [15]	2DCLML [19]	PROPOESD (E-Type)
Num. of Switches	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	N_L+3	N_L+1	N_L+1	N_L+1	N_L-1	$5(N_L-1)/6$
Num. of Diodes	N_L+1	$2(N_L-1)$	$2(N_L-1)$	N_L+3	N_L+1	N_L+1	N_L+1	$7(N_L-1)/3$	$5(N_L-1)/6$
Num. of DC links	$(N_L-1)/2$	(N_L-2)	$(N_L-1)/2$	$(N_L-1)/2$	$(N_L-1)/2$	$(N_L-1)/2$	$(N_L-1)/2$	$(N_L-1)/3$	$(N_L-1)/3$
TSV* (xV_{DC})	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$3(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$10(N_L-1)/6$
Negative level	With at least Two arms	With at least Two arms	With H-Bridge	With H-Bridge	With H-Bridge	With H-Bridge	With H-Bridge	inherent	inherent
Num. of switches in terms of DC links	4	2+ $2/(N_L-2)$	4	1/3+ $4/3(N_L-1)$	2+ $4/(N_L-1)$	2+ $4/(N_L-1)$	2+ $4/(N_L-1)$	3	5/2
PIV** in terms of DC source	4	2+ $2/(N_L-2)$	4	6	4	4	4	6	5

* Total Standing Voltages **Peak Inverse Voltage

III. SELECTIVE HARMONIC ELIMINATION MODULATION METHOD

Selective harmonic elimination modulation (SHE-PWM) method is utilized in this paper to create pulse pattern for the proposed inverter. In this method, as shown in Fig.5, different angles ($\alpha_1,\ldots,\alpha_6$) are calculated to form a staircase multilevel waveform with the lowest possible THD. The method is implemented based on optimization techniques where each desired harmonic order can be eliminated. Selection of switching angles for a multilevel converter is presented in [21-22] using a phase-shift harmonic suppression approach. Generally, SHE-PWM is based on the Fourier series decomposition of the periodic PWM voltage waveform and calculation of the switching angles (α_i) in order to eliminate selected low harmonic orders. Fourier series of a periodic function can be written as:

$$f_n(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n \sin(2\pi nt/T) + b_n \cos(2\pi nt/T)) \quad (1)$$

As $f_n(t)$ is odd, the equation can be rewritten as:

$$f_n(t) = \sum_{n=1}^{\infty}(b_n \cos(2\pi nt/T) \quad (2)$$

Where b_n as follows, v is step level voltage:

$$b_n = \frac{4v}{n\pi}\sum_{i=1}^{i} \sin(n\alpha_i) \quad (3)$$

In the proposed topology, as shown in Fig.3, there are 6 voltage levels in quarter-wave symmetry and therefore 6 switching angles (α_i) have to be calculated. Third harmonic multiples are eliminated in three phase systems. Thus 9th and 15th harmonics are not considered in the equations. It helps to consider more harmonic components in equations for elimination (such as 17th and 19th instead of 9th and 15th). 3rd is just considered for its higher amount in equations in single phase [23] systems to reduce THD%. To eliminate 3th, 5th, 7th, 11th, 13th, 17th and 19th harmonic orders, (4) have to be solved in order to achieve α1 to α6 with the condition of $0<\alpha1<\alpha2<\alpha3<\alpha4<\alpha5<\alpha6<\pi2$. Table III shows the results for the degree of each step level with m_a varies from 0 to 1 with 0.01 variations. The below equations are used in Particle Swarm Optimization (PSO) Algorithm and Differential Evolution (DE) Algorithm to generate the Optimized angles to Eliminate Selected Harmonics, Those are shown below table III and IV respectively.

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$$\begin{cases} b_1 = \frac{4V}{1\pi}[\cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)+\cos(\alpha_4)+\cos(\alpha_5)+\cos(\alpha_6)] \\ b_3 = \frac{4V}{3\pi}[\cos(3\alpha_1)+\cos(3\alpha_2)+\cos(3\alpha_3)+\cos(3\alpha_4)+\cos(3\alpha_5)+\cos(3\alpha_6)] = 0 \\ b_5 = \frac{4V}{5\pi}[\cos(5\alpha_1)+\cos(5\alpha_2)+\cos(5\alpha_3)+\cos(5\alpha_4)+\cos(5\alpha_5)+\cos(5\alpha_6)] = 0 \\ b_7 = \frac{4V}{7\pi}[\cos(7\alpha_1)+\cos(7\alpha_2)+\cos(7\alpha_3)+\cos(7\alpha_4)+\cos(7\alpha_5)+\cos(7\alpha_6)] = 0 \\ b_{11} = \frac{4V}{11\pi}[\cos(11\alpha_1)+\cos(11\alpha_2)+\cos(11\alpha_3)+\cos(11\alpha_4)+\cos(11\alpha_5)+\cos(11\alpha_6)] = 0 \\ b_{13} = \frac{4V}{13\pi}[\cos(13\alpha_1)+\cos(13\alpha_2)+\cos(13\alpha_3)+\cos(13\alpha_4)+\cos(13\alpha_5)+\cos(13\alpha_6)] = 0 \\ b_{17} = \frac{4V}{17\pi}[\cos(17\alpha_1)+\cos(17\alpha_2)+\cos(17\alpha_3)+\cos(17\alpha_4)+\cos(17\alpha_5)+\cos(17\alpha_6)] = 0 \\ b_{19} = \frac{4V}{19\pi}[\cos(19\alpha_1)+\cos(19\alpha_2)+\cos(19\alpha_3)+\cos(19\alpha_4)+\cos(19\alpha_5)+\cos(19\alpha_6)] = 0 \end{cases}$$

--- (4)

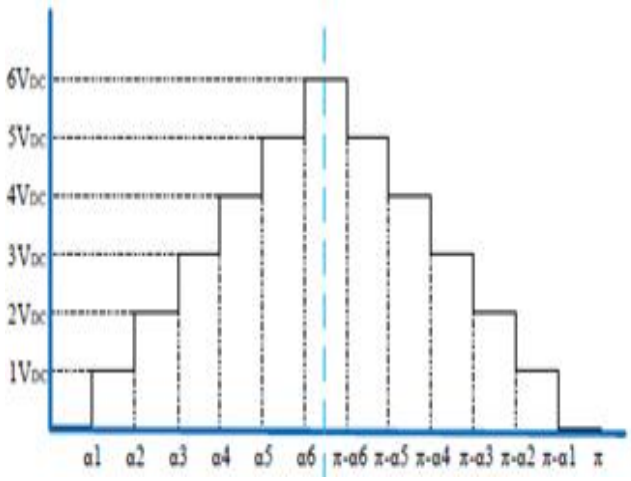

Fig.5 Wave form of selective harmonic elimination to find α_i (Quarter wave symmetry)

TABLE III
DEGREE OF EACH STEP LEVELWITH $m_a = 0\ to\ 1$ by PSO at $C_1 = 1$ and $C_2 = 3$

α_i	α_1	α_2	α_3	α_4	α_5	α_6	THD
Degree	5.2899	16.2725	22.2859	33.6120	49.0228	63.1949	3.15%

TABLE IV
DEGREE OF EACH STEP LEVELWITH $m_a = 0\ to\ 1$ by DE at CR=0.8 and F=0.5

α_i	α_1	α_2	α_3	α_4	α_5	α_6	THD
Degree	5.3201	16.2308	22.3235	33.5857	49.0247	63.1779	3.14%

The Convergence graphs of THD vs Number of iterations for the PSO and DE Algorithms are shown in below fig.6 and fig.7 re-

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spectively.

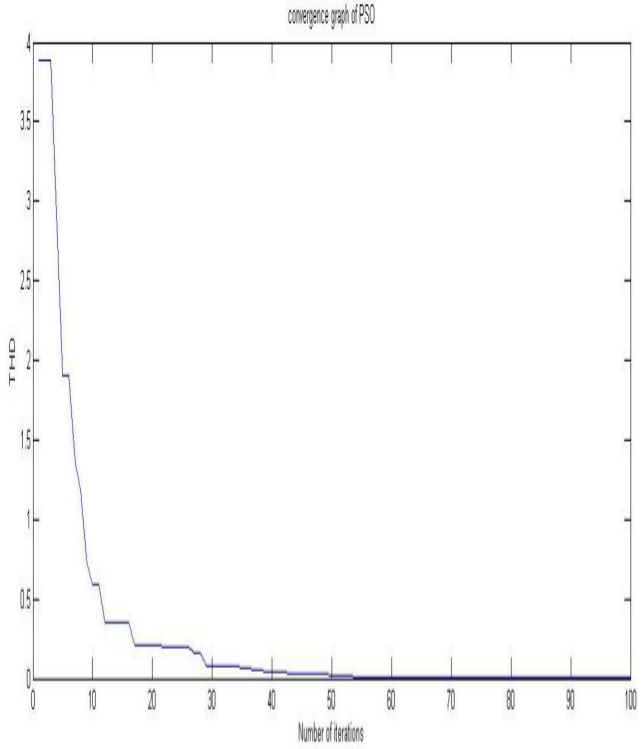

Fig.6.Convergence graph for PSO

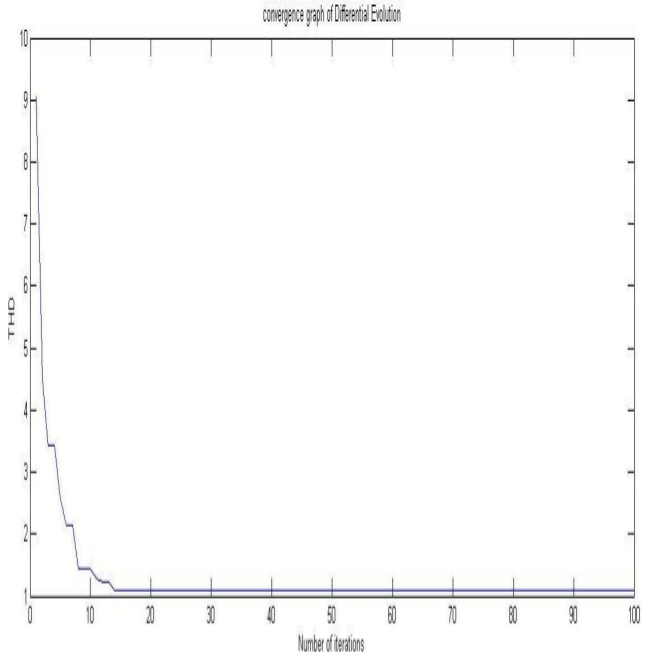

Fig.7.Convergence graph for DE

IV. SIMULATION CIRCUIT

The Simulation Circuit for the Proposed Topology is shown in the below fig.8 and Control logic for switching pattern of proposed model is shown in below fig.9.

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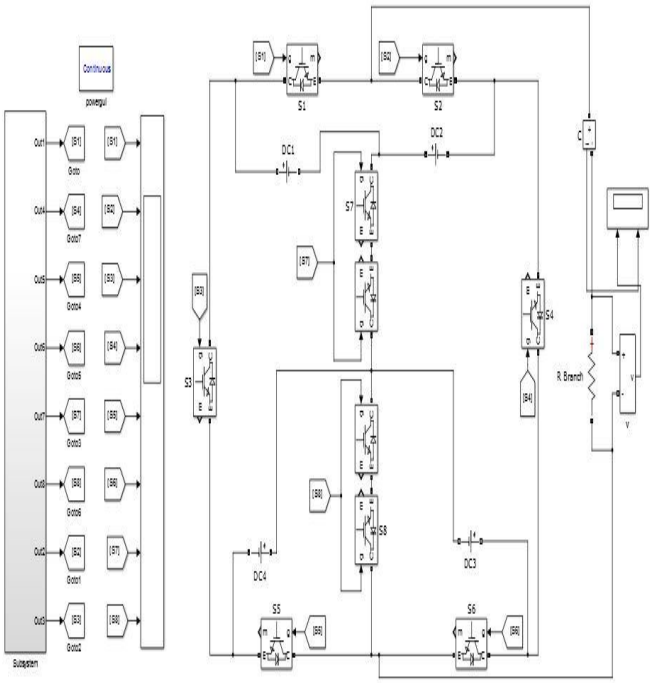

Fig.8.Simulink model for Proposed Circuit

V. EXPERMENTAL RESULTS

The proposed multilevel module is simulated by using MATLAB to examine the performance of proposed module. Fig.9 shows the output voltage of 13-levels (Each level is 50 volts) of the proposed multilevel inverter with SHE modulation switching method with 3.15% THD by using PSO Algorithm and 3.14% by using Differential Evolution (DE) Algorithm. FFT analysis is shown in below fig.10 and fig.11. And comparison table for Newton Raphson (NR), PSO and DE methods are shown in Table V. It satisfied IEEE 519 (i.e. max. of THD%: 8%, max. of THD for each order: 5%). Here considered voltage sources are two 50V and two 100V and Resistance(R)=150ohms.

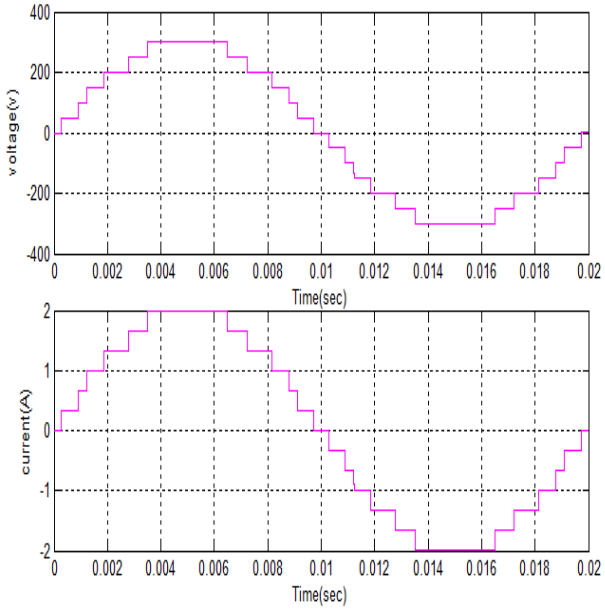

Fig.9.Thirteen level inverter output voltage and current waveforms for PSO and DE method

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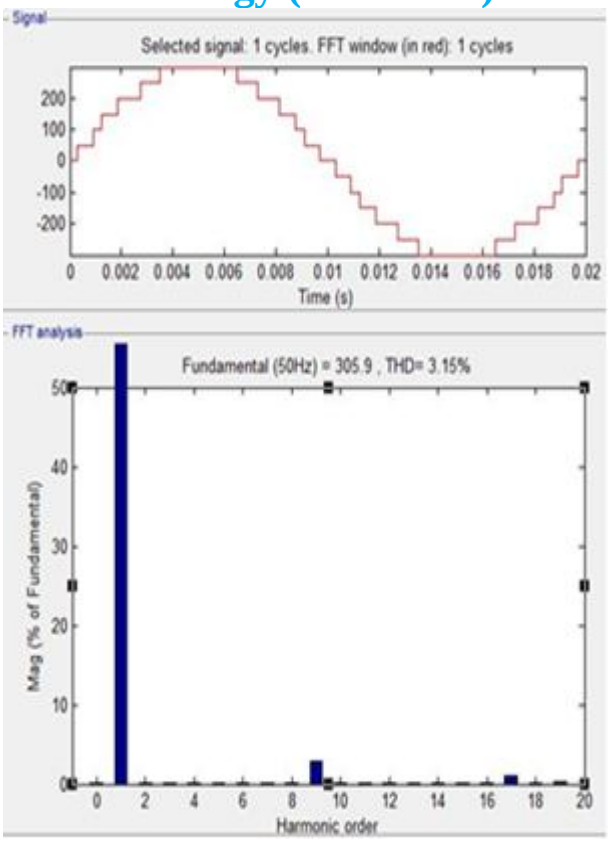

Fig.10 Output voltage and FFT analysis of proposed multilevel by using DE Algorithm

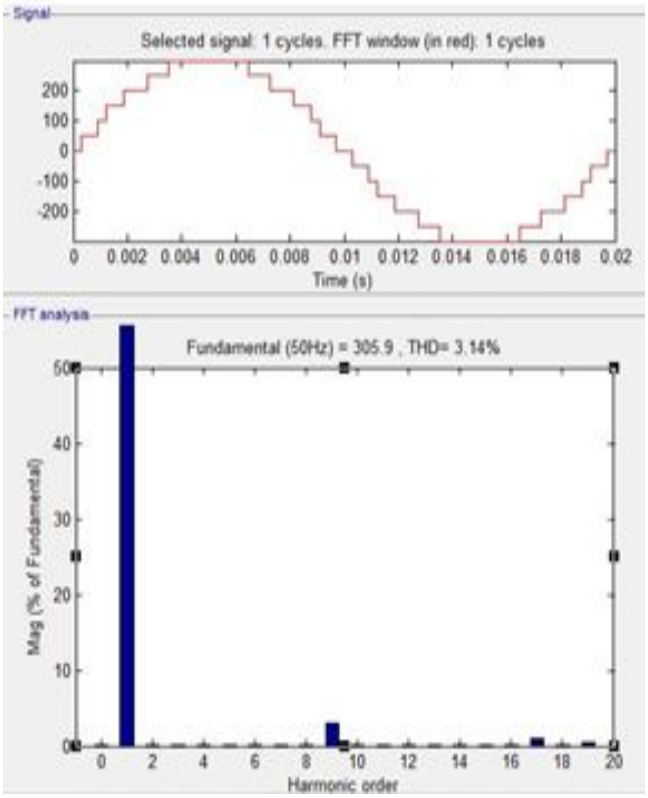

Fig.11 Output voltage and FFT analysis of proposed multilevel by using DE Algorithm

TABLE V
COMPARISON OF PULSE WIDHHS FOR NR, PSO AND DE METHODS

α_i	α_i	α_i	α_i	α_i	α_i	α_i	THD
Degree	4.9183	16.2842	26.2549	31.1794	51.2926	64.5696	5.24%
Degree	5.2899	16.2725	22.2859	33.6120	49.0228	63.1949	3.15%
Degree	5.3201	16.2308	22.3235	33.5857	49.0247	63.1779	3.14%

NR-Newton Raphson Method

VI. CONCLUSION

This paper presented a new multilevel inverter module which can generate 13 levels with less number of components. It can be used in high voltage high power applications with unequal DC sources. This module can be easily modularized; it can be used in cascade arrangements to form high voltage outputs with low stress on semiconductors and lowering the number of devices. Modular connection of these modules leads to achieve more voltage levels with different possible paths. It causes an improvement in the reliability of the modular inverter which enables it to use different paths in case of malfunction for a switch or a driver. The main advantage of proposed module is its ability to generate both positive and negative output voltage without any H-bridge circuit at the output of the inverter. THDv% is obtained 3.15% and 3.14% for PSO and DE methods respectively And comparison different methods to generate pulse widths are shown in table V. The simulation results are satisfying harmonics standard (IEEE519).

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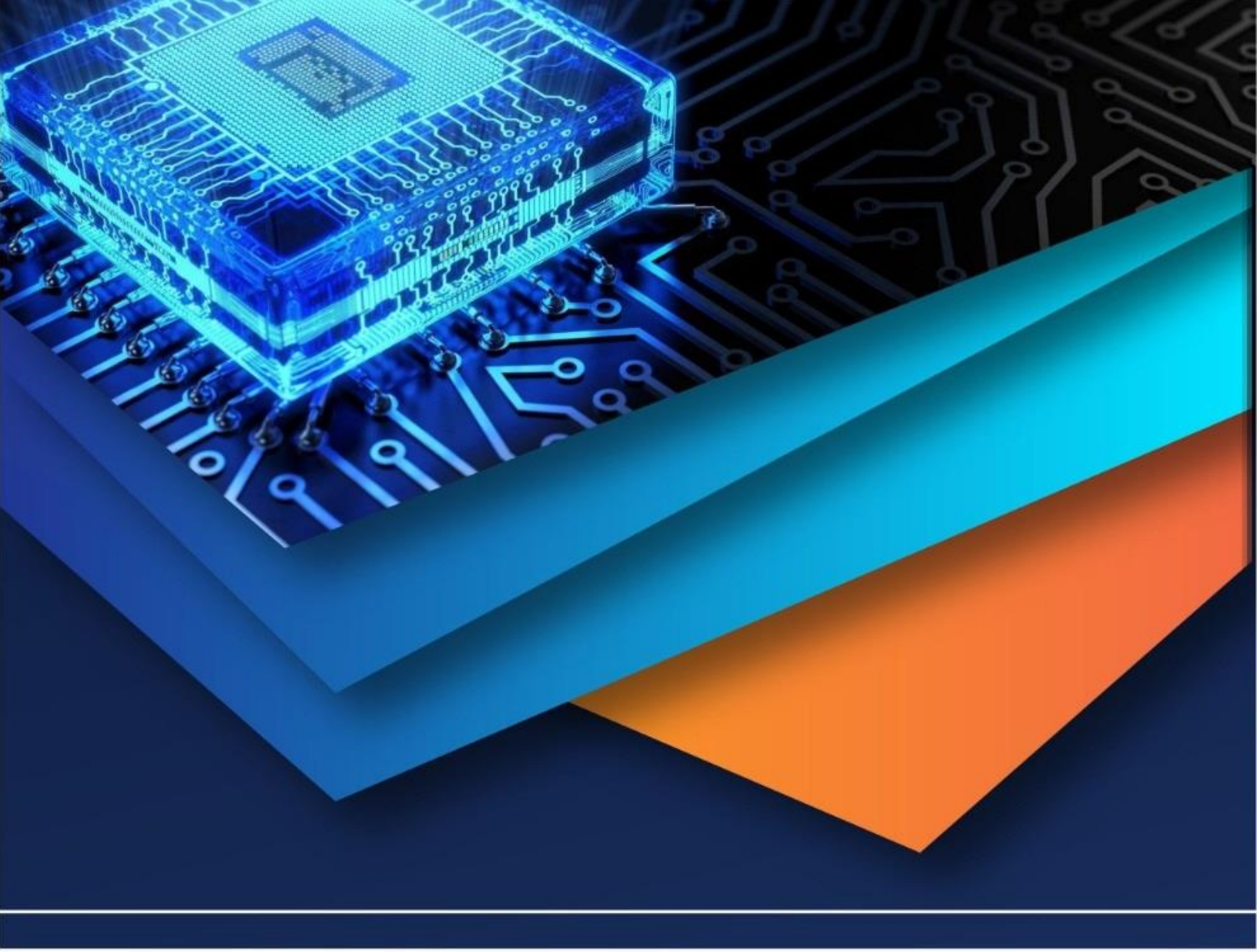

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