iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** V **Month of publication:** May 2017

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Analysis of Efficient Adiabatic Logic Circuits and Their Power Extraction in Finfet (10nm) and Comparison With 90nm and 45nm

Sunnivesh Suman[1], M. Murali Krishna[2], I. Sreenivasa Rao[3]
[1,2,3] *Electronics and Communication, Gitam University*

***Abstract**: This paper describes the design style and analysis of low power adiabatic logic circuits based on ECRL (Efficient Charge Recovery Logic Circuits), PFAL(Positive Feedback Adiabatic Logic) and SCRL(Split Charge Recovery Logic).These logic families always functions based on four phase power clock. These designs have the proficiency of energy saving by recycling or reusing the certain amount of the energy, which helps in reduction of power dissipation. This paper describes how the power and delay factor depends on the timing analysis. "CADENCE" virtuoso has used for the design of energy saving adiabatic circuit. In the analysis, three nanometer technologies have compared. This paper shows that how the power and delay vary as the frequency is increased. In the analysis, ECRL, PFAL and SCRL technologies also have compared. It has found that adiabatic circuits are superior for low power applications.*

Keywords: Adiabatic Techniques, Efficient Charge Recovery Logic (ECRL), Positive Feedback Adiabatic Logic (PFAL), Split Charge Recovery Logic (SCRL), Power Clock, Low Power System.

I. INTRODUCTION

With the development in the miniaturization of the MOS in the VLSI technology, chips are designed to have transistors in the higher numbers. According to the use, the designers increase or decrease the number of transistors. Today there are lakhs of transistors on the single chip. These transistors make the circuits small and small which help in designing the portable devices. Today the portable devices are high in use like power bank, mobile, ipod, other medical gadgets like pacemakers etc. These portable devices run on battery. The circuits are designed by taking care of battery so that the battery does not drain much and the life of the device be more. These circuits are designed in CMOS where the power dissipation is at the cost of efficiency in speed. The CMOS devices operate at high speed but at the cost of high power dissipation. As the number of transistors increase it will cost to the power efficiency in CMOS. Thus, Adiabatic CMOS has been introduced. The adiabatic CMOS is a CMOS design only but have different design specification. In the CMOS design, if it is required to decrease the power dissipation, it is necessary to play with the supply voltage, capacitance associated with the design and switching factor. But in the adiabatic CMOS it is not like this. In the Adiabatic CMOS, the power dissipation can be decreased by tuning the timing analysis. This will be discussed in the further section. The different logic styles which has discussed are ECRL, PFAL, SCRL. It has also shown what will happen if the adiabatic circuits are designed in the FINFET.

Section 2 describes the adiabatic logic and adiabatic switching.
Section 3 describes the how adiabatic switching is different from adiabatic switching.
Section 4 describes the different adiabatic logic families

II. ADIABATIC LOGIC AND ADIABATIC SWITCHING

Adiabatic is the terminology, which has taken from the thermodynamics. It is defined as the process where no energy exchange with the environment and hence no power dissipation [1]. It says that adiabatic system never takes or dissipates the energy from the environment. It is the energy, which is developed inside the system during the process and after the completion of the work, the energy recovered by the system. This property of the adiabatic logic makes it more popular towards the designer. The adiabatic circuits uses oscillating clock[2]in the power supply. This means that in place of giving the constant supply voltage, the ramp supply voltage is introduced in the design. The ramp supply voltage will limit the energy dissipation in the circuit. To understand this we need an RC network circuit with the ramp supply[3].

Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

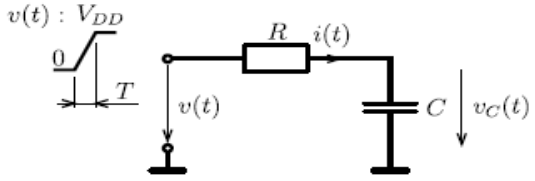


Fig1. Circuit to determine the losses by adiabatically loading a capacitance

In the given circuit, the resistance R path is used to charge the capacitor. The ramp voltage input has given to the ciruit.
The energy dissipation is given by

$$E_{dissp} = I(t) * Vdd\,(t) \quad [4]$$

The current flowing through the RC circuit is given by

$$i(t) = C\frac{dv(t)}{dt} = \frac{CV_{dd}}{T} \quad [5]$$

The energy is calculating by integrating the power with respect to the time taken by the capacitor to charge.

$$E = \int_0^T p(t)dt$$

$$= \int_0^T v(t) * i(t)dt$$

$$= \int_0^T (v_r(t) * v_c(t)) * i(t) \quad [5]$$

The integral of Vc(t) · i(t) over one clock cycle will be zero, as no energy is dissipated in the capacitance. Thus by replacing the voltage Vr(t) with i(t)*R in equation. Thus, the energy dissipation of the adiabatic circuit is given as

$$E = \int_0^T R\frac{C^2Vdd^2}{T^2}dt = \frac{RC}{T}CVdd^2$$

As from the above adiabatic energy dissipation equation it is understood that the energy is the factor of R, C, Vdd, T. The energy dissipation can decrease by lower the resistance and capacitance. The resistance and capacitance are directly proportional to the energy dissipation. But the problem with the this is that the resistance and capacitance has the lower limit. Below that limits we cannot decrease the energy.
Since, Time 'T' is inversely proportional to the energy dissipation, the power can be reduced in the effective manner.
For lower the Energy dissipation,T> 2RC. As the time is more than the 2RC, the less energy dissipation will occur.

III. ANALYSIS OF CONVENTIONAL SWITCHING AND ADIABATIC SWITCHING

To understand the conventional switching, let's take CMOS inverter.

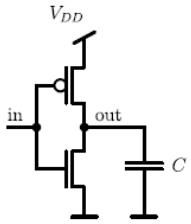


Fig2: CMOS Inverter

In the CMOS inverter, the capacitance is charged through the supply source. In the static CMOS the capacitor is charged through the switching process. When input transition 1 to 0 is applied, the PMOS transistor turns on and NMOS turns off. The path for the charge is from supply source to capacitor. A charge Q=C.Vdd flows to the capacitor. So the total energy taken from the supply

Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

source is

$$E_{cmos} = Q.Vdd$$
$$E_{cmos} = C.Vdd^2 \quad [6]$$

During the PMOS on, the energy stored at the capacitor is

$$E_{cmos} = \frac{1}{2} C.Vdd^2 \quad [6]$$

The half of the energy is dissipated during the charging process. As the input transition switches from 1 to 0, the PMOS off and NMOS becomes on. The path is created between output and ground. The energy stored at the capacitor will dissipate through this path. So the total energy dissipation in the static CMOS is given by

$$E_{cmos} = \alpha . C.Vdd^2 \quad [6]$$

Where α is the switching factor, C is the capacitance, Vdd is the supply voltage. To reduce the energy dissipation, the different steps has taken. The switching factor has reduced to minimum number so that the dissipation be minimum. But the switching factor is a design phenomenon which has the lower limit beyond which we can not decrease the energy. Similarly we scale the capacitor and supply voltage. The voltage scaling has done as Vdd is directly proportional to E. From the above equation it has shown that inverter has the lower limit of $\frac{1}{2} C.Vdd^2$. This makes the adiabatic CMOS more beneficial over the static CMOS. As in adiabatic CMOS, the lower limit depends on the T. As the T increases the energy dissipation will be more lower.

IV. DIFFERENT ADIABATIC LOGIC FAMILY

A. *Effective Charge Recovery Logic*

Effective Charge recovery logic is quasi-adiabatic logic. It is also called the partial adiabatic logic. The ECRL consists of the two cross-coupled PMOS which drives the N-functional block and /N functional block. The power clock supply is provided to the circuits which recycle or reuse the energy stored in different phase of the clock. The clock is divided in the four phases: Evaluation Phase, Hold Phase, Recovery Phase and wait Phase. In the ECRL, the pre-charge and the evaluation phase occurs simultaneously.[7] Full output swing is obtained because of cross-coupled PMOS transistors both in the pre-charged and recovery phase. This circuit suffers from non-adiabatic loss.[7]

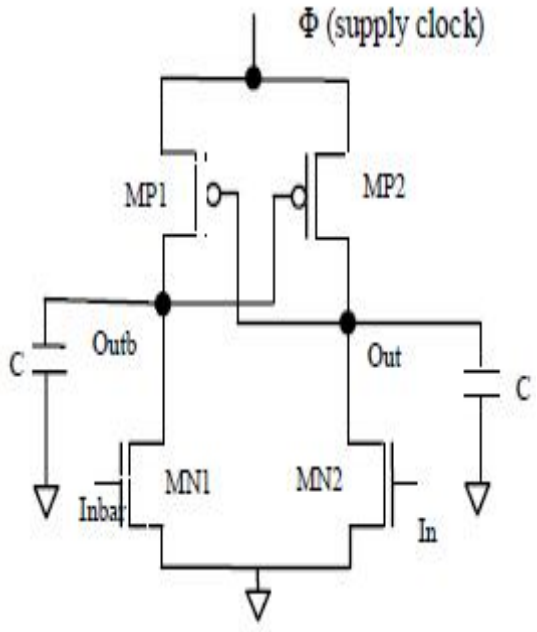


Fig3 ECRL

The ECRL circuit has dual input signals and dual output signals. The out and /out are generated so that the power clock generator can always drive a constant load capacitance.

Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

1) Positive Feedback Adiabatic Logic

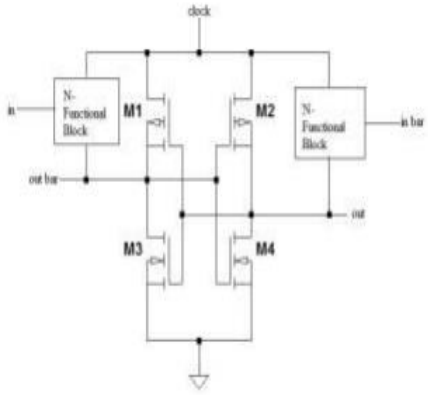


Fig4. Positive Feedback Adiabatic Logic

Positive Feedback Adiabatic Logic (PFAL) shows the lowest energy consumption compared to other partial logic technique and a good robustness against technological parameter variations. The latch made by two PMOS M1-M2 and two NMOS M3-M4 that avoids a logic level degradation on the output nodes. The two N-functional blocks are placed parallel to PMOS transistor and it forms a transmission gate. The latch is made by two PMOS transistors and two NMOS transistors, and the functional blocks are in parallel with the transmission PMOS transistors. Thus the equivalent resistance is smaller when the capacitance needs to be charged.

2) Split Charge Recovery Logic

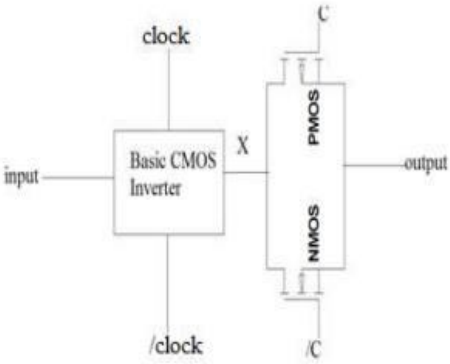


Fig 5: Split Charge Recovery Logic

Scrl uses as many devices as conventional CMOS. It requires only one wire for every signal. It drives all output during sampling. It is identical conventional CMOS except that it uses pass transistor logic at the output. The SCRL inverter consists of one PMOS and one NMOS with time varying supply and also an additional transmission gate at the output. The basic CMOS inverter have two complementary power clocks „clock" and „/clock" rather than Vdd and ground terminals. The power clock varies between Vdd and Vdd/2 whereas /clock varies between Vdd/2 and 0. Initially all the nodes (clock and /clock) are at Vdd/2, at this time the transmission gate is turned OFF by the control signals C and /C. The output is also at Vdd/2. After applying valid input the transmission gate at the output is gradually turned ON by swinging C and /C to Vdd and ground respectively. Clock and /clock also swing to Vdd and ground respectively. If the input to the gate is Vdd then the node x and the output will follow /clock and ground but if the input was at ground the node x and output follow /clock and Vdd.

V. PROPOSED DESIGN

Adiabatic Logic has designed in the FINFET to study the power analysis and delay factor. This shows that how the efficiency of the circuit increases in the FINFET rather than 90nm and 45nm. The SG mode FINFET technology has used to design the adiabatic logic. In shorted-gate (SG) FinFETs, the two gates are connected together, leading to a three- terminal device. This can serve as a

Volume 5 Issue V, May 2017
ISSN: 2321-9653

direct replacement for the conventional bulk-CMOS devices.

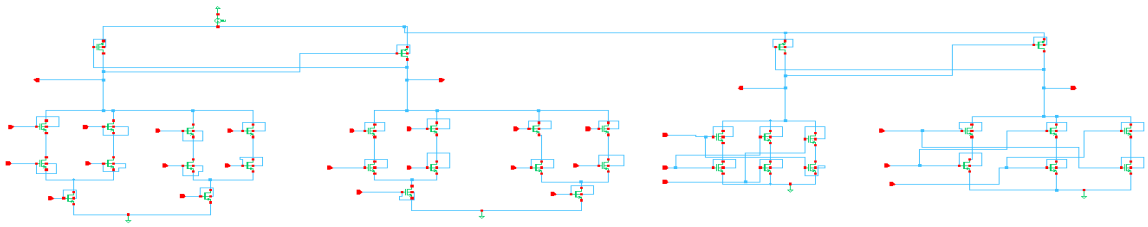


Fig4. SG MODE ECRL FULL ADDER

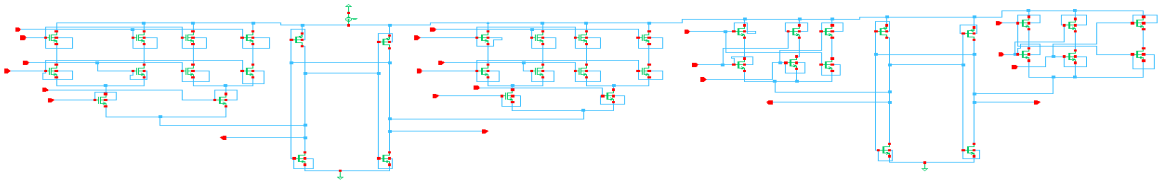


Fig5. SG MODE PFAL FULL ADDER

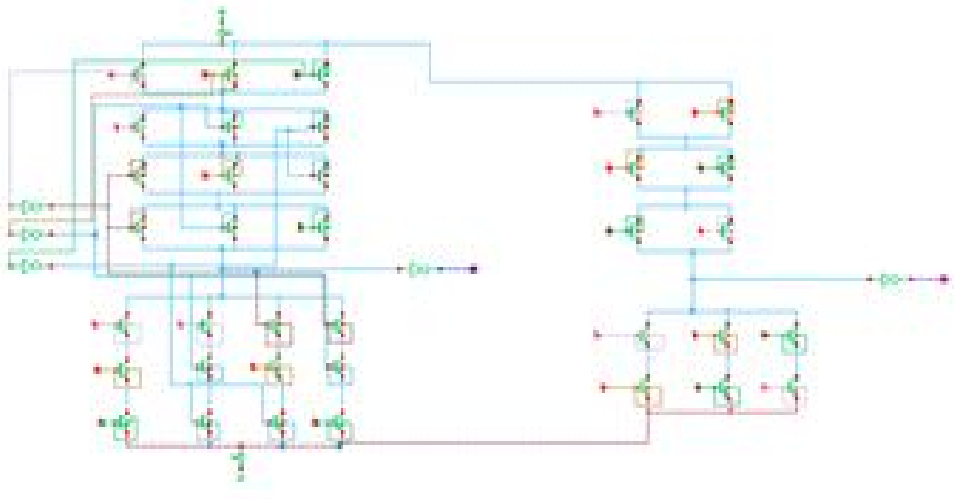
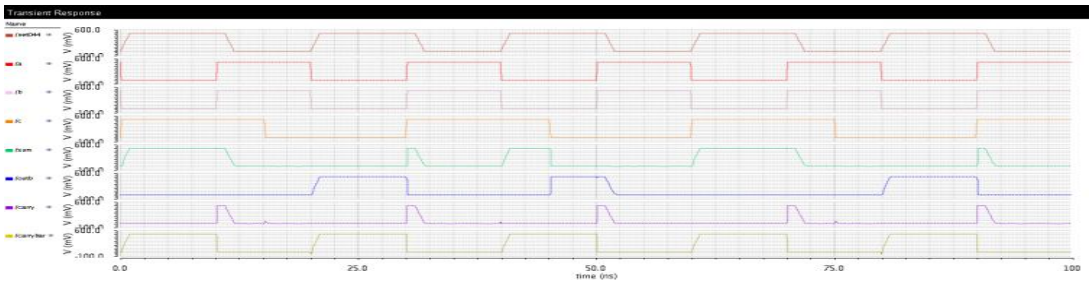


Fig6. SG MODE SCRL FULL ADDER

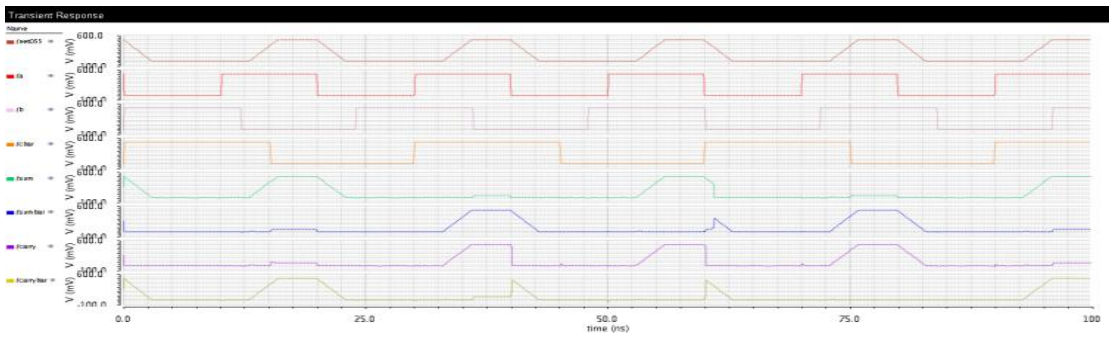
The above design of 1-bit full adder has done in 10nm SG-Mode FINFET. The adiabatic logic has also designed in 90nm and 45nm.

Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

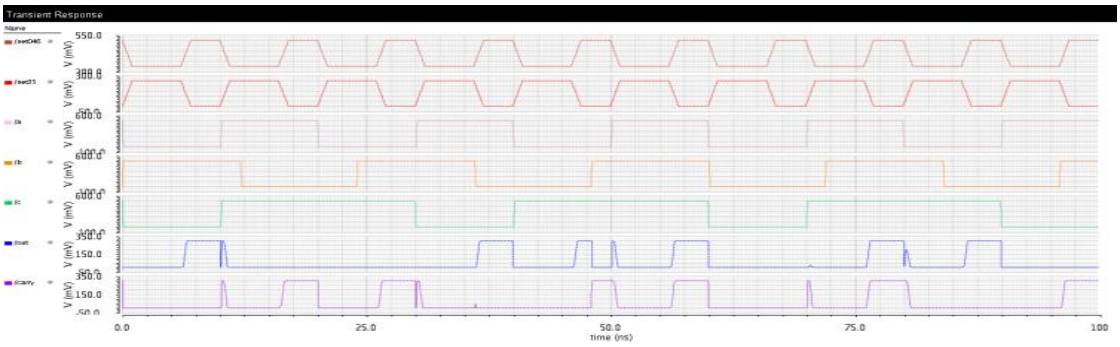
VI. RESULTS AND DISCUSSION



Graph1: full adder ECRL



Graph2 : full adder PFAL



Graph3: full adder SCRL

POWER(W)	1ns	3ns	5ns	6ns
ECRL	1.231e-6	671.1e-9	320.9e09	197.9e-9
PFAL	2.083E-10	1.811E-10	847.5E-11	545.08E-11
SCRL	246.5E-9	145.5E-9	145.8E-9	48.61E-9

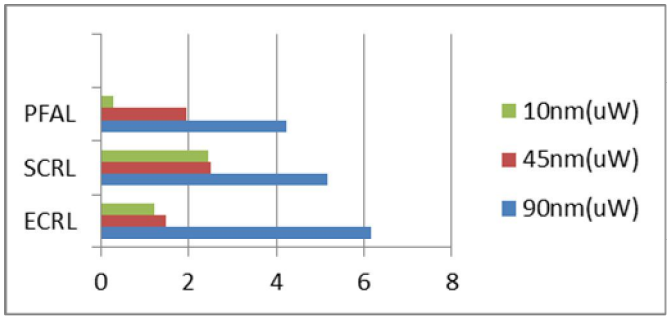
Table 1: Power Analysis with respect to Time 'T'

Delay(sec)	1ns	3ns	5ns	6ns
ECRL	1.350e-9	4.348e-9	7.340e-9	8.838e-9
PFAL	1.351E-9	4.349E-9	7.348E-9	8.848E-9
SCRL	433.8E-12	434.3E-12	435.8E-12	436.9E-12

Table 2: Delay Analysis with respect to time 'T'

Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

VII. COMPARISON OF 90NM AND 45NM TO FINFET

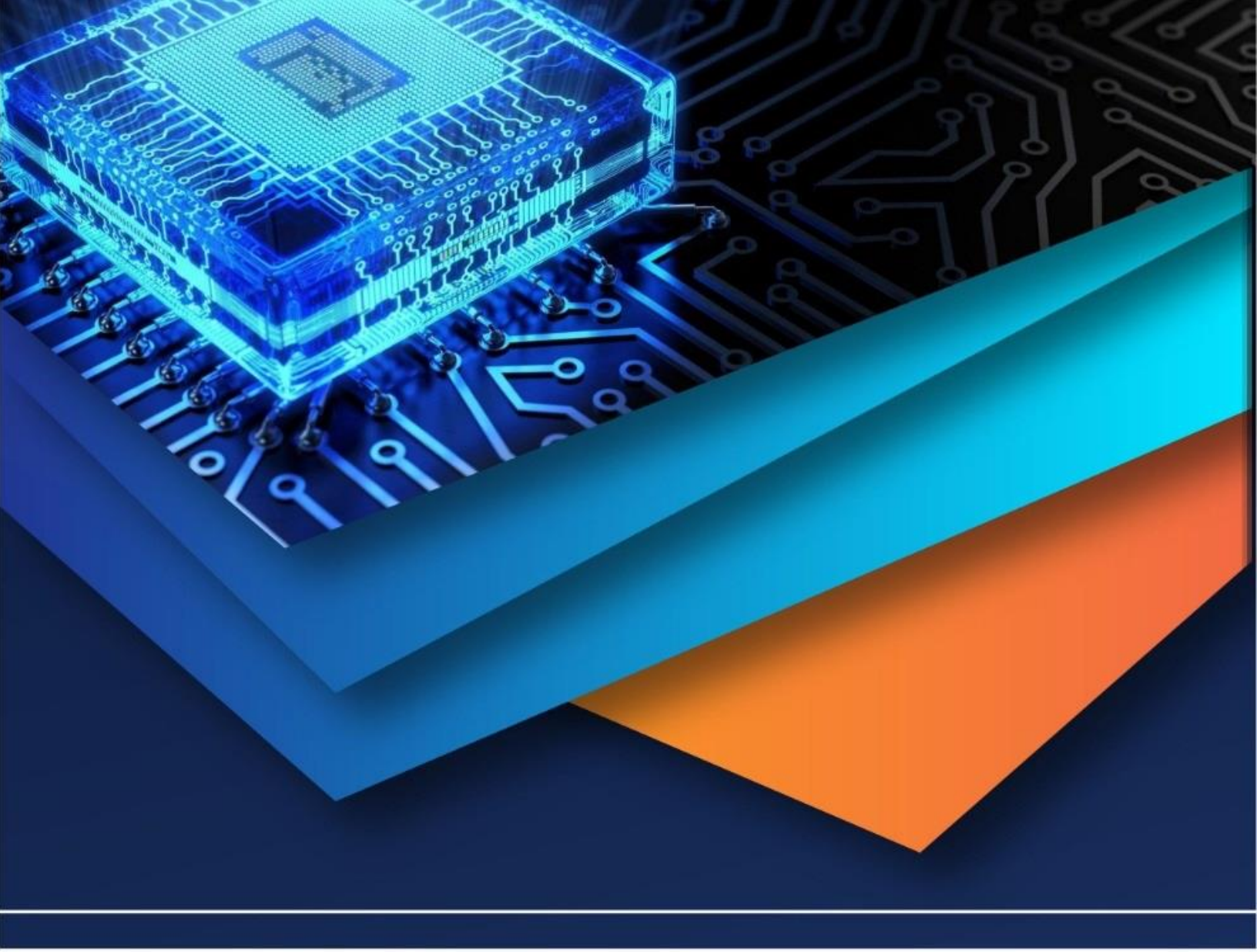


VIII. CONCLUSION

The design of adiabatic circuits in the FINFET has the much more advantage. its efficiency regarding the power dissipation has increased. In the adiabatic logic, the power dissipation can be controlled in terms of varying the timing slope. To achieve less power, increase the ramp of the power clock which leads to slow charging of the capacitor. But in the adiabatic process, the less power is achieved at the trade-off of speed. The delay of the circuit increases as the ramp of the clock increases. PFAL logic has more accuracy among all.

REFERENCES

[1] J.S. Denker "A review of adiabatic computing," In: IEEE Symposium on Low Power Electronics, San Diego, 1994. 94–97.
[2] Nikhil Deo1, Rusni Kima Mangang, Kumar Murugan3," Power Gating in FinFET Adiabatic Circuits" In: Green Computing Communication and Electrical Engineering (ICGCCEE), 2014 International Conference by IEEE
[3] Y. Moon, and D.-K. Jeong, "An Efficient charge recovery logic circuit," IEEE J. of Solid-State Circuits, vol. 31, no. 4, pp. 514–522, 1996.
[4] Philip Teichmann "Adiabatic Logic Future Trend and System Level Perspective", ISSN 1437-0387 Springer Series in Advanced Microelectronics ISBN 978-94-007-2344-3 e-ISBN 978-94-007-2345-0 DOI 10.1007/978-94-007-2345-0 Springer Dordrecht Heidelberg London New York.
[5] William C. Athas, Lars "J." Svensson, Member, IEEE, Jeffrey G. Koller, Nestoras Tzartzanis, and Eric Ying-Chin Chou, Student Member, IEEE, "Low-Power Digital Systems Based on Adiabatic3 witching Principles", IEEE TRANSACTIONS ON VERY LARGF SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 2, NO. 4, DECEMBER 1994.
[6] William C. Athas, Lars "J." Svensson, Member, IEEE, Jeffrey G. Koller, Nestoras Tzartzanis, and Eric Ying-Chin Chou, Student Member, IEEE, "Low-Power Digital Systems Based on Adiabatic3 witching Principles", IEEE TRANSACTIONS ON VERY LARGF SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 2, NO. 4, DECEMBER 1994.
[7] L. G. Heller and W. R. Griffin, "Cascode voltage switch logic: A differential CMOS logic family," Proc. IEEE International Solid-State Circuits Conference, 1984, 16-17.
[8] Munish Mittal, Anil Khatak , " Design and Analysis of Energy Recovery Logic for Low Power Circuit Design", International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 National Conference on Advances in Engineering and Technology (AET- 29th March 2014)
[9] Simranjeet Singh Puaar, Sandeep Singh Gill, "POWER EVALUATION OF ADIABATIC LOGIC CIRCUITS IN 45NM TECHNOLOGY",INTERNATIONAL JOURNAL OF ELECTRONICS AND COMMUNICATION ENGINEERING & TECHNOLOGY (IJECET), Volume 5, Issue 12, December (2014), pp. 230-237.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY