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Design of 12-Bit DAC Using CMOS Technology

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Abstract: ***Digital-to-Analog Converter (DAC) is used to convert a digital form of input into an analog form of output. In this paper, a digital-to-analog converter which is based on the R-2R ladder is analyzed for low power consumption i.e. 27.04 mW, low active chip area i.e. .054 mm^2 and low DNL i.e. 0.03. R-2R DAC is implemented using cadence virtuoso tool in 180nm CMOS process. The main components used are an operational amplifier and R-2R ladder network. Op-amp is made up of two stages. The first stage of op-amp consists of a differential amplifier and the second stage consists of common source amplifier. The first stage is used to get high gain and the second stage increases output swing and gain of the first stage.***
Keywords: operational amplifier; CMOS; R-2R ladder; DNL; DAC

I. INTRODUCTION

An R-2R Ladder is a basic and sensible method for performing digital to analog transformation. R-2R ladder comprises of an arrangement of resistors in ladder-like structure. It changes over a parallel digital input into an analog output voltage. Individual digital input (B0, B1, B2, and so forth.) includes its own particular weighted commitment to the analog output yield.

A. The features of this network

1) It can be easily designed for any number of bits
2) This DAC uses only two values of resistors.
3) The output impedance of this DAC is fixed i.e. R, irrespective of a number of resistors [1].

Resistance ladder or resistor string converter is a basic type of DAC. This DAC comprises of resistor string of indistinguishable resistors, and parallel switch exhibit whose sources of input are the binary word. The simple output is the voltage division of the resistors streaming through pass switches. The output is associated with at most N switches on and N turns off [2]. In this paper, 12-bit digital input (D0 to D11) is converted into analog output V_{dac}. The supply voltage used is 2.5V and the technology used is CMOS 180nm process. Voltage step for N-bit DAC can be expressed as in equation (1)

$$\Delta v = \frac{Vdac}{2^N} \quad (1)$$

For a 12-bit DAC, the value of output voltage will change in steps of 0.6mV. In R-2R ladder DAC, nonlinearity occurs for resistor ladder network as they do not create regular resistance values.

It is very difficult to construct resistor based DAC with high resolution because it requires a large number of resistors. A better choice will be the use of R-2R ladder configuration. Fig 1 shows the basic block diagram of 12-bit DAC.

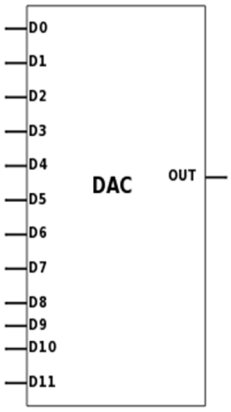

Fig 1: Basic block diagram of 12-bit DAC

The design here is a 12-bit R-2R architecture DAC implemented using cadence virtuoso tool in 180nm CMOS technology. The

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main features of the 12-bit R-2R DAC design are discussed in the next sections. In Section II an overview of the design of the DAC is discussed. In Section III obtained simulation results and waveforms are presented. The main conclusion result is presented in Section IV.

II. DAC DESIGN

In this work, a 12-bit digital to analog converter is designed. The implementation of 12-bit R-2R DAC is shown in Fig 2. An R-2R resistor network and an operational amplifier are the major components used to build the circuit.

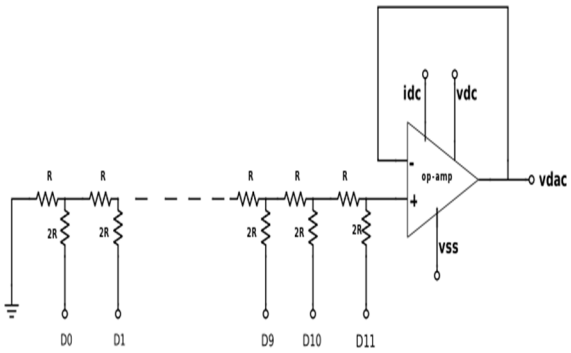

Fig 2: Implementation of 12-bit R-2R DAC

A. *Design of op-amp*

An op-amp is an amplifier having high gain and input impedance which is used to perform mathematical operations on an input voltage. This op-amp consists of two stages namely differential amplifier stage and common source stage. The schematic of the op-amp is shown in Fig3. The inputs given for op-amp are idc 5µV, Vdd 2.5V, Vss -2.5V, vninv gnd and vinv is given Vsin pulse with amplitude 5mV and frequency 1k. Finally, the output is taken from transient, AC and dc analysis. Gain and bandwidth of op-amp are also calculated.

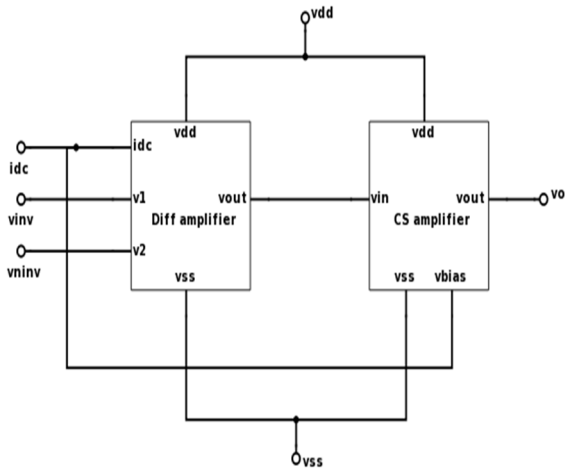

Fig 3: Schematic of op-amp

B. *Design of differential amplifier*

A differential amplifier is an electronic amplifier which amplifies the difference between two input voltages and suppresses the common voltage. The differential amplifier is the first stage in designing op-amp. This stage is used to get high gain. The schematic of the differential amplifier is shown in Fig4. The inputs given for differential amplifier are idc 5µV, Vdd 2.5V, Vss -2.5V, vninv gnd and vinv is given Vsin pulse with amplitude 5mV and frequency 1k. Finally, the output is taken from transient, AC and dc analysis.

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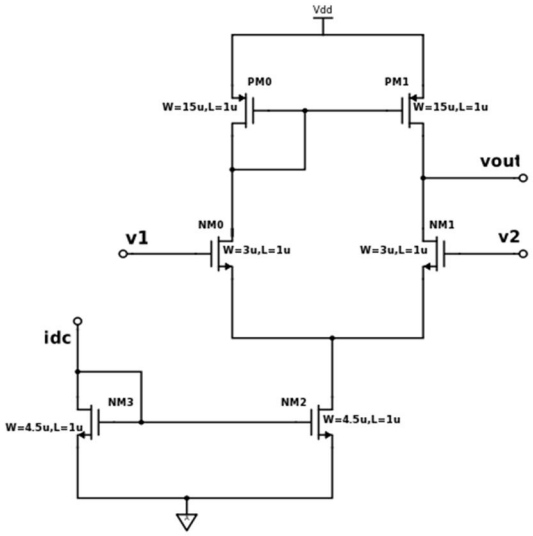

Fig 4: Schematic of the differential amplifier

C. Design of CS amplifier

Common source amplifier is the second stage used in the design of op-amp. This stage is used to improve gain and output swing of the first stage i.e. differential stage. The schematic of cs amplifier is shown in Fig5. The inputs given for cs amplifier are idc 5µV, Vdd 2.5V, Vss -2.5V, vninv gnd and vinv is given Vsin pulse with amplitude 5mV and frequency 1k. Finally, the output is taken from transient, AC and dc analysis.

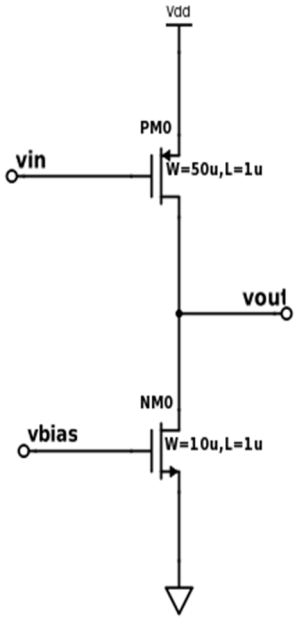

Fig 5: Schematic of CS amplifier

III.SIMULATION RESULTS AND WAVEFORMS

A. DAC output

To obtain the output of DAC, its transient analysis has been done. The input value of idc is 5µV and Vdd is 2.5V. Simulation result

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of 12-bit R-2R DAC is shown in Fig 6.

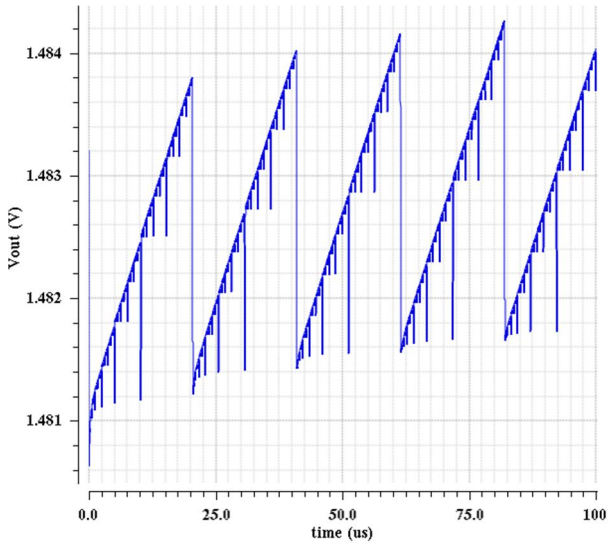

Fig 6: Simulation result of 12-bit R-2R DAC

B. DAC layout

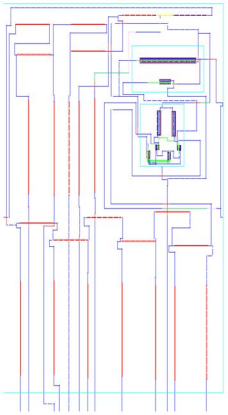

Fig 7: Physical layout of 12-bit R-2R DAC

C. DAC parameters

DAC parameters like power consumption, area, delay and DNL has been calculated as shown in TABLE I.

TABLE I
DAC PARAMETERS

Parameters	[10]	[9]	This work
Technology (µm)	0.13	0.18	0.18
Resolution (bits)	12	12	12
Supply voltage (V)	0.72-1.2	1.8	1.8-2.5
Power consumption (mW)	13.4	48.6	27.04
Area (mm^2)	0.072	-	0.054
DNL	0.7	0.6	0.03

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IV. CONCLUSIONS

A 12-bit R-2R DAC is designed and implemented in cadence virtuoso tool using 180nm CMOS process. This DAC is designed for low power consumption, low active chip area, and low DNL. As compared to previous work in 180nm technology, power is reduced from 48.6 to 27.04mW and DNL is reduced from 0.6 to 0.03. Comparing from 130nm technology, DNL is reduced from 0.7 to 0.03 and active chip area is reduced from 0.072 to 0.054mm^2.

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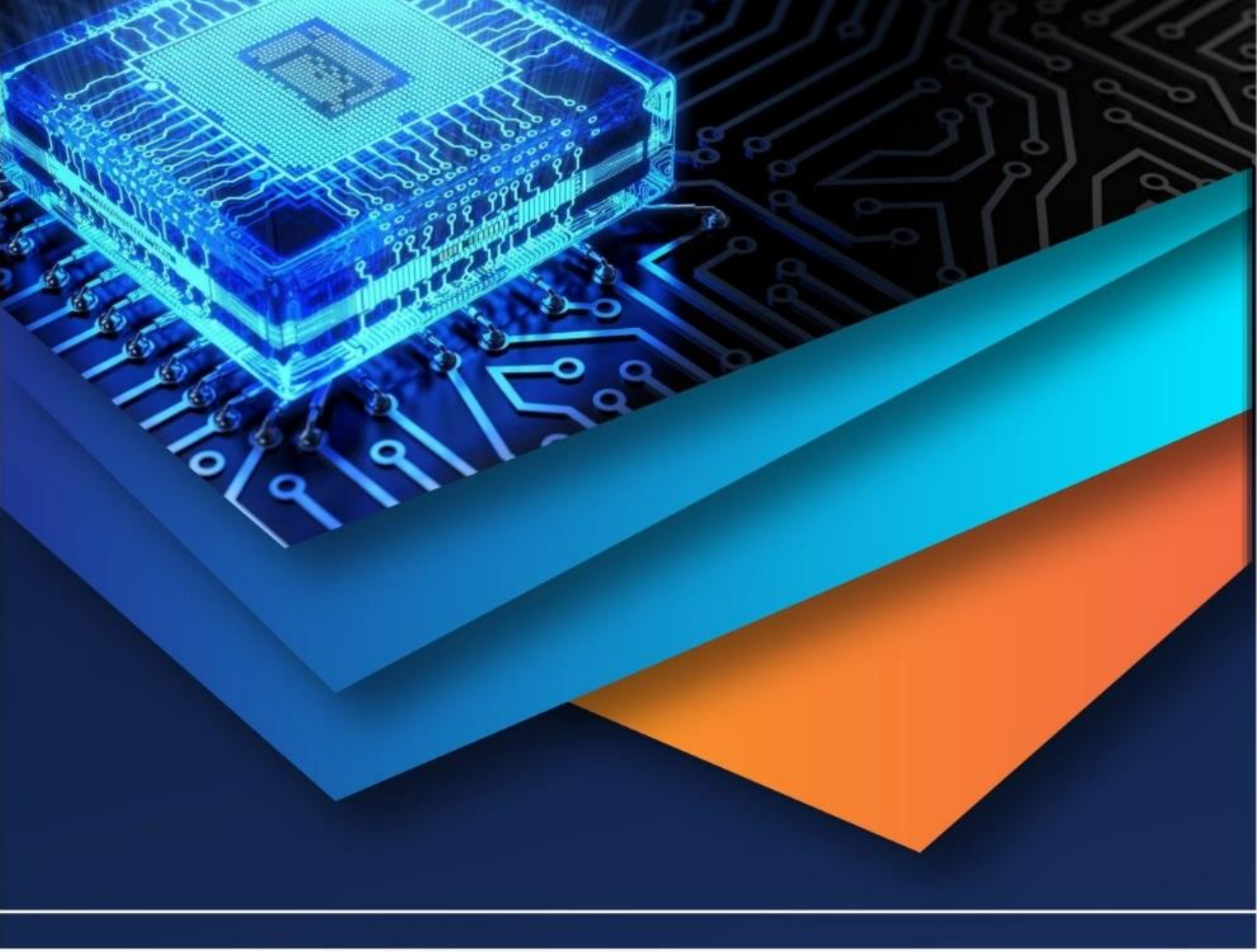

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