iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VI **Month of publication:** June 2017

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Quantum Realization Full Adder-Subtractor Circuit Design Using Islam gate

Madhumita Mazumder[1] , Indranil Guha Roy[2]
[1,] *Computer Science & Engineering Dept, West Bengal University of Technology*
[2]*Information Technology Dept, Manipal University*

Abstract: ***Quantum Computing is one of the emerging computing methods of future computing technologies. The construction of quantum computer that performs computation is implemented using Quantum Gate, the basic gate level element. Due to its quantum nature, the Quantum Gates are reversible but it different from the classical reversible gate. As all operations are reversible, the reversible circuits form the basic building block of quantum computers. In my previous work [15], Islam Gate (IG) which is the 4*4 parity preserving reversible gate, was implemented using quantum gate CNOT, NOT, Toffoli, Swap gate and Peres gate. That implementation was used to construct a Full Adder quantum circuit using Islam Gate. In this work, a proposed reversible and quantum realization of Full Adder-Subtractor circuit is implemented using quantum representation of Islam (IG) Gate [15] circuit.***

Keywords: Classical Circuit, Quantum computing, Quantum Circuit, Reversible Logic, Reversible Gates.

I. INTRODUCTION

In last few decades, the advancement of the IC fabrication technology increased the counting of components IC exponentially [1]. According to Moore's law [2], this number is doubling every 18 months and hence the components are reduced to atomic level, thereby increasing the heat dissipation during computation and affecting the performance of the processor. According to Landauer's Principle [2], for every bit of irreversible operation, kTlog2 joules amount of heat is generated that goes into computing environment. When components of IC reduced atomic level computing process fails to do next generation computation, the quantum physics helps to continue the same. So for future, reversible computation [3] and quantum computation [4] are most important methods of computation. Reversible Gate [5] is the basic gate level element of reversible computing and 4*4 Islam Gate (IG) is a reversible gate. This Islam Gate was implemented using quantum gates[15] and Quantum Full Adder Circuit was implemented by Quantum representation of Islam Gate[15].Here it is possible to show that a quantum full adder-substractor can also be implemented using this technique.

II. BACKGROUND

A. Reversible Gate

A gate or a circuit is called reversible if the number of inputs is equal to number of outputs; i.e. a reversible gate performs only permutation of its input vectors. If a reversible gate has k inputs and k outputs, then it's called a k*k reversible gate, like Fig 1. A k*k gate is said to have width k and there is (2k)! possible reversible gates of width k. The term Reversibility in computing implies that information about the computational states cannot be lost. So it is possible to recover earlier stage outcomes by computing backwards or un-computing the results. This is called as logical reversibility [4], which can be gained only after employing physical reversibility. The term Physical reversibility is a process that dissipates no energy to heat. Practically perfect physical reversibility is not possible to achieve.

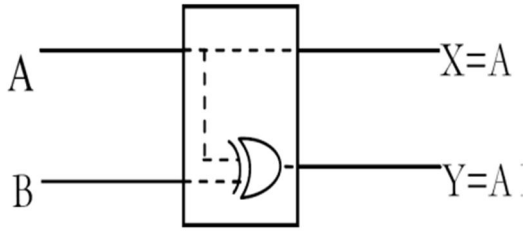


Fig. 1 Reversible XOR gate

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

B. Quantum Gate

In quantum circuit model of computation, a quantum logic gate is a basic quantum circuit, operating on a small number of qubits. Like classical logic gate AND is for conventional digital circuits, Quantum logic gate is the building block of quantum circuits. But classical logic gates are not reversible. However, classical computing can also be implemented by
using reversible gates. For example, the reversible Toffoli gate can implement all Boolean functions. This gate has a direct quantum equivalent, showing that quantum circuits can perform all operations performed by classical circuits. Some quantum gates are shown in Fig 2.

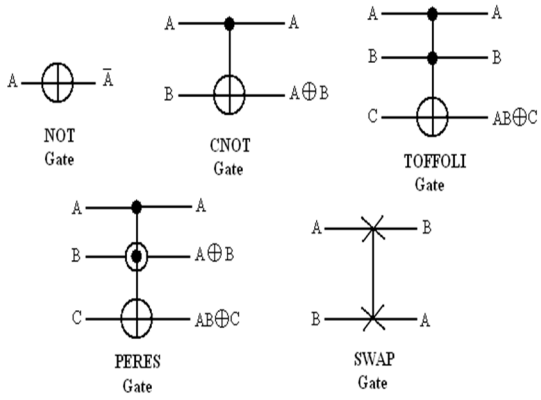


Fig 2: Quantum Gates

C. Combinational full adder and full subtractor circuit and truthtable

Circuit that consists of only digital logic gates and where the output at any point of time is determined by the present input combinations, without taking into consideration of any previous or old instances of inputs, is called combinational circuit. Adder, Subtractor etc is the classic examples of such combinational circuits as introduced in Fig 3 and 4.

To perform the summation of the bits, the most common and widely used circuit is Adder. Likewise the most common subtraction operation is performed by Subtractor.

Full adder performs addition of three bits i.e. X, Y and Z and output S, denoting summation and C denoting carry, are shown in Table I. Same two input bits as a full adder along with an extra bit for an incoming carry can also be used in full adder to perform addition operation.

Similarly full subtractor performs subtraction of three bits i.e. A, B and Din and output Difference and Bout, denoting borrow. Same two input bits as a full subtractor along with an extra bit for an incoming borrow can also be used in full subtractor to perform subtraction operation. Truth table of combinational full subtractor is shown in Table II.

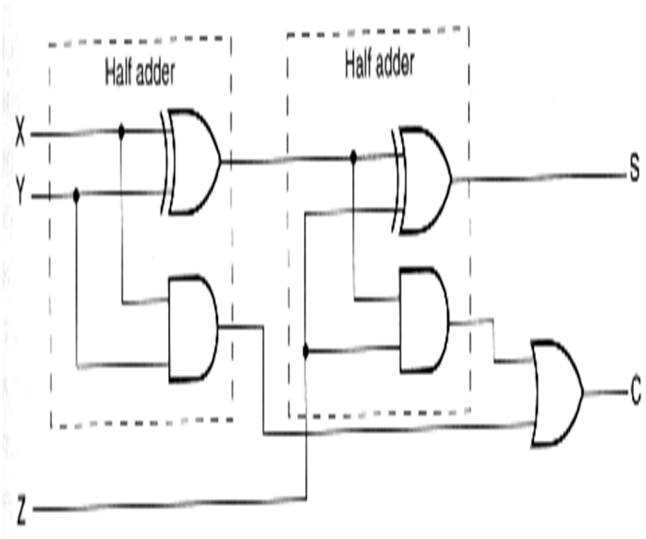


Fig3 Classical Full Adder circuit

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

TRUTH TABLE OF CLASSICAL FULL ADDER CIRCUIT

input			output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

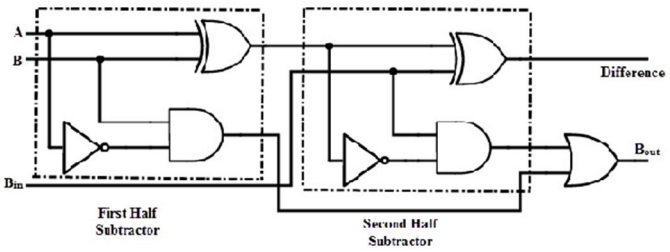


Fig 4 Classical Full Subtractor Circuit

TABLE I. TRUTH TABLE OF CLASSICAL FULL SUBTRACTOR CIRCUIT

input			output	
A	B	Din	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

D. Reversible Islam Gate & its Quantum Representation

In paper [5] a 4*4 parity preserving Islam gate was described and the same is shown below in Fig 5. This can readily be verified by comparing the input parity A B C D to the output parity P Q R S. The IG gate is universal in the sense that it can be used for implementing arbitrary Boolean functions.

Quantum Realization of 4*4 Islam Gate is shown in Fig 6. This quantum circuit for Islam Gate is implemented with Toffoli Gate, CNOT Gate, NOT Gate, Swap Gate and Pares Gate [15]. G1 is Garbage value; A, B, C, D are the Inputs and P, Q, R, S are the respective Outputs. Using RC viewer+ simulator ,Simulation was successfully done on quantum realization of Islam gate using both of +ve and also –ve controlled Toffoli Gate(TG) to find out the quantum cost of quantum represented of Islam gate(IG) , as Fig 7 and 8 [15]. The Quantum Cost of quantum Islam Gate Circuit with Negative control TG is 18 and total Gate count is 5, as Fig 9 [15]. The truth table of Islam gate is shown in Table III. RC Viewer+ always give the result in reverse sequence in case of truth table shown in Fig 10.

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

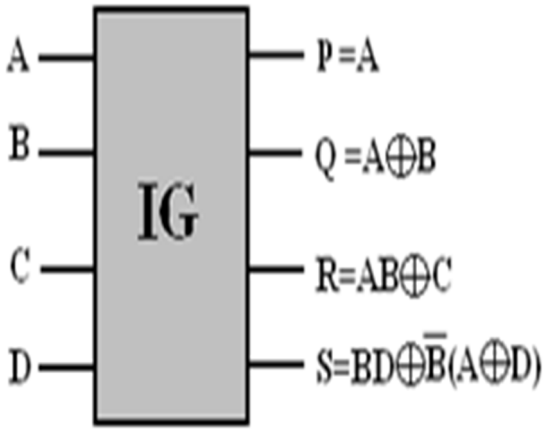


Fig 5 4*4 Parity Preserving Reversible Islam Gate

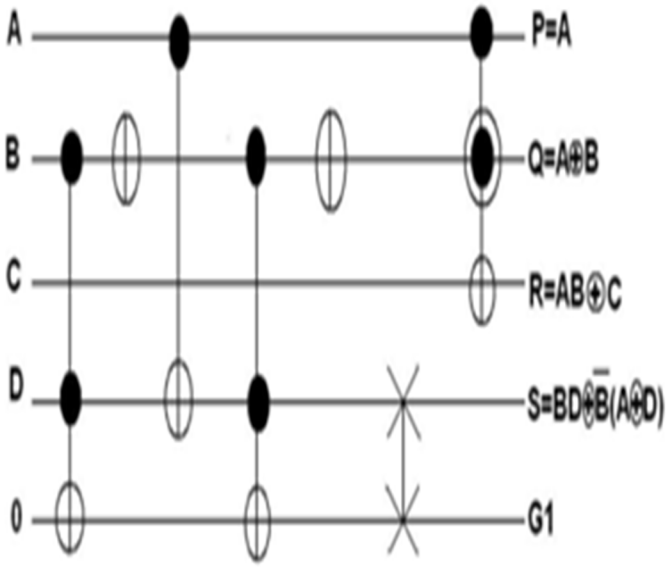


Fig 6 Quantum Circuit for Islam Gate

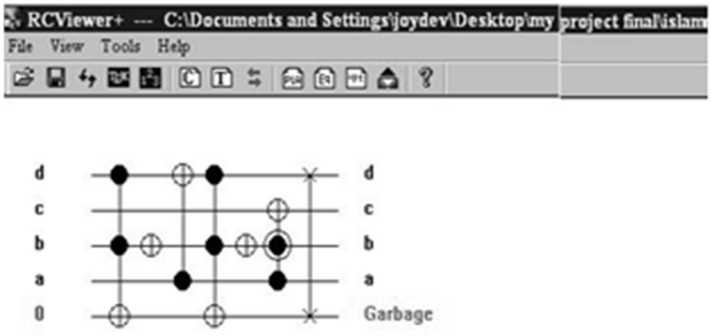


Fig.7 Quantum Ckt for Islam Gate (with positive control TG) in RC-Viewer+

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

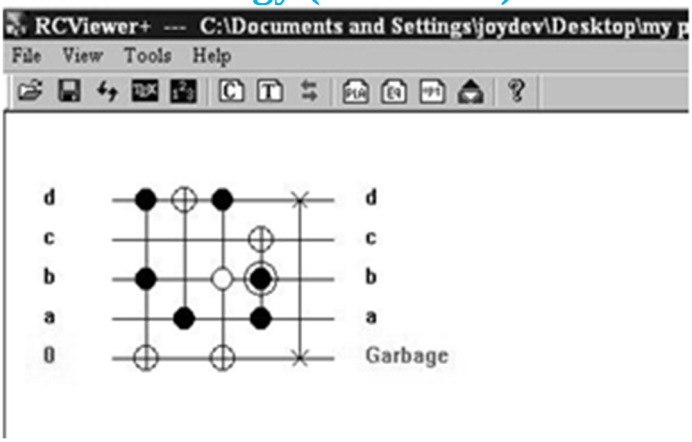


Fig.8 Quantum Ckt for Islam Gate (with negative control TG)in RC-Viewer+

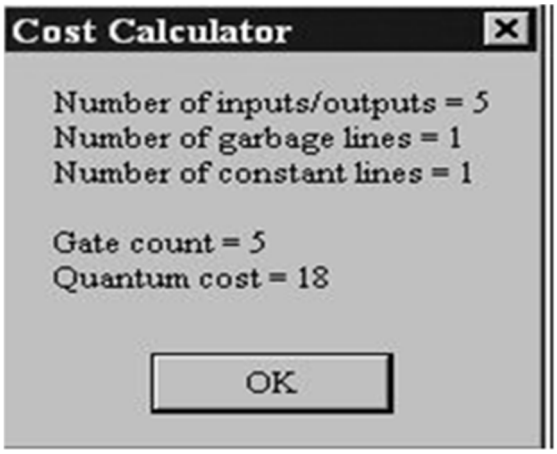


Fig 9: Quantum Cost of Islam Gate with negative Control TG.

TABLE II. TRUTH TABLE FOR ISLAM GATE WITHOUT SIMULATION

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

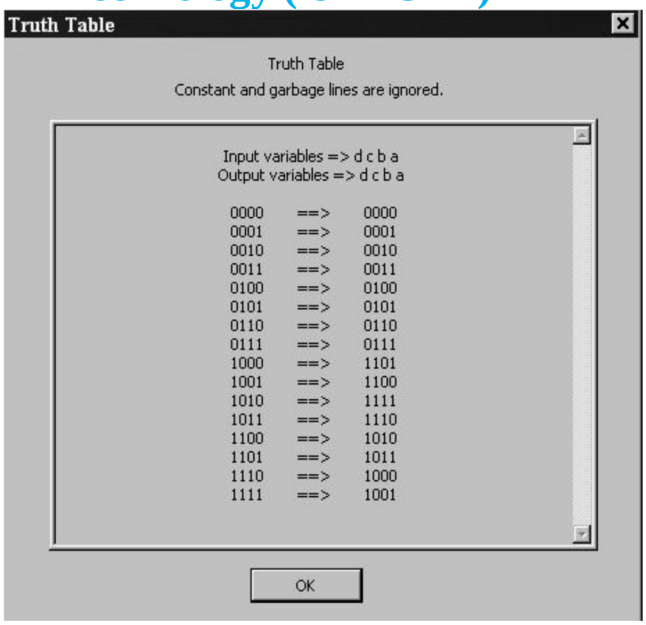


Fig 10 Truth table for Islam Gate after simulation

III. PROPOSED CIRCUIT

A. Reversible Circuit for full adder-subtractor Circuit using reversible Islam Gate

The proposed Reversible circuit for full adder-subtractor using 4*4 reversible Islam Gate is introduced here where S/D represents both summation and difference. Carry and borrow, both can also be found in the circuit. Three Islam gates (4*4 reversible) are used to design this proposed reversible Full adder-subtractor circuit, as shown in Fig11.

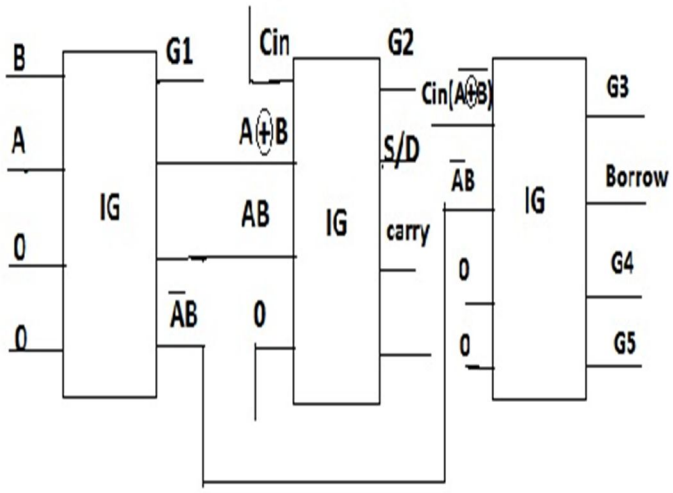


Fig 11 Proposed Reversible Full Adder-Subtractor Circuit

B. Proposed Quantum Circuit for Full Adder-subtractor

In the previous section, established the minimum number of garbage outputs and constant inputs required to design a fault tolerant reversible full adder circuit [5] and then proposed a realization of fault tolerant reversible full adder circuit using the newly proposed parity preserving 4*4 reversible gate IG and that is efficient than the existing designs. Fig 8 and Fig 9 shows the Quantum Realization of Islam Gate circuit [15] with both positive and negative control Toffoli Gate. Now A Quantum circuit with both full Adder and Subtractor , is implemented by 3 Islam gate (IG) quantum circuit and find the sum/Difference ,carry and borrow, are shown in Fig 12. Sum/Differnce, Carry and Borrow. From G1 to G8 are all Garbage value.

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

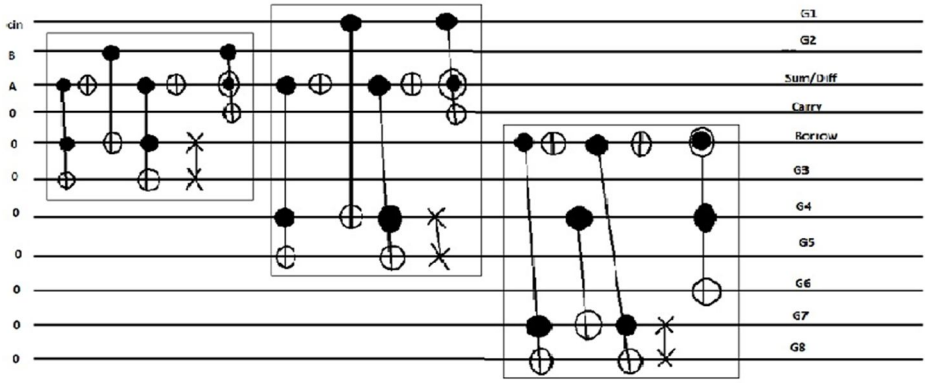


Fig 12 Proposed Quantum Representation of Full Adder-Subtractor circuit using 3IGs.

IV. SIMULATION & RESULT

This proposed quantum circuit is implemented using RCViewer+ (Version 2.31). To calculate quantum cost, the sum of the quantum costs of its gates is calculated. Quantum cost depends on number of garbage value, number of constant value and cost of each gate**.**

A. Proposed Quantum Full Adder-Subtractor Circuit

The proposed quantum representation of Full Adder-Subtractor circuit is designed by three quantum Islam Gate circuits and it's shown in Fig 13. To Reduce the cost, it is possible to use quantum Islam Gate with negative control Toffoli gate as shown in Fig14, where r=>Sum/Difference, s=>Carry, t=>Borrow.

If we use negative control in this proposed circuit Through 3 quantum Islam gate (IG) with negative Control, the quantum cost will be reduced, because two CNOT is replaced by negative control in each quantum circuit for IG. So, total six number of CNOT is replaced with unit cost. In Fig 14, proposed circuit with negative control TGs is more efficient than previously discussed proposed circuit with positive control TGs shown in Fig.13, if we calculate the cost of proposed quantum Full Adder-Subtractor circuit.

In the Truth table, as shown in Fig 15,the result will introduced in reverse order of output veriable sequence(r s t),that Means it will encounter from right to left as per the properties of RCViewer+ simulator.

After decomposing the proposed circuit into primitive gates, the result will be, as shown in Fig 16.

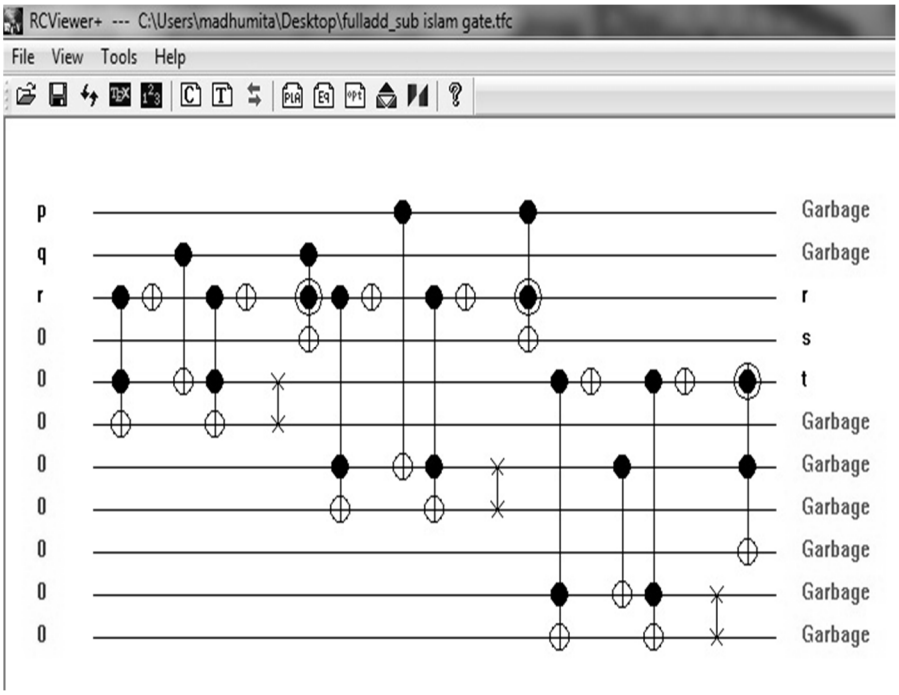


Fig 13 Proposed Quantum Representation of Full adder-Subtractor circuit using 3IGs (with +ve control TG).

Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

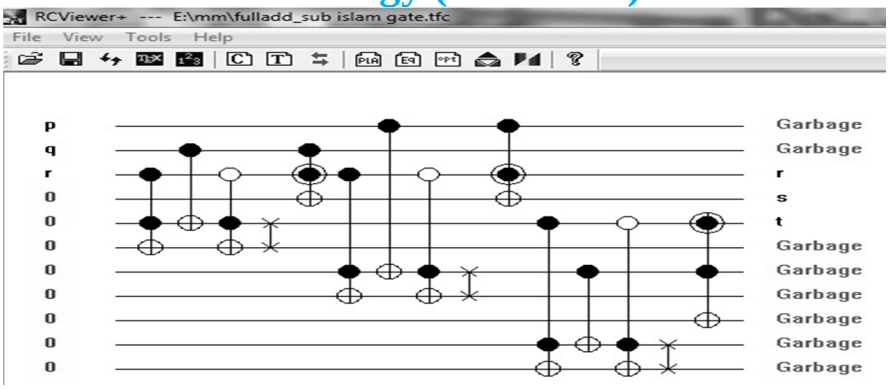


Fig 14 Proposed Quantum Representation of Full Adder-Subtractor using 3IGs (with a negative controlled TGs).

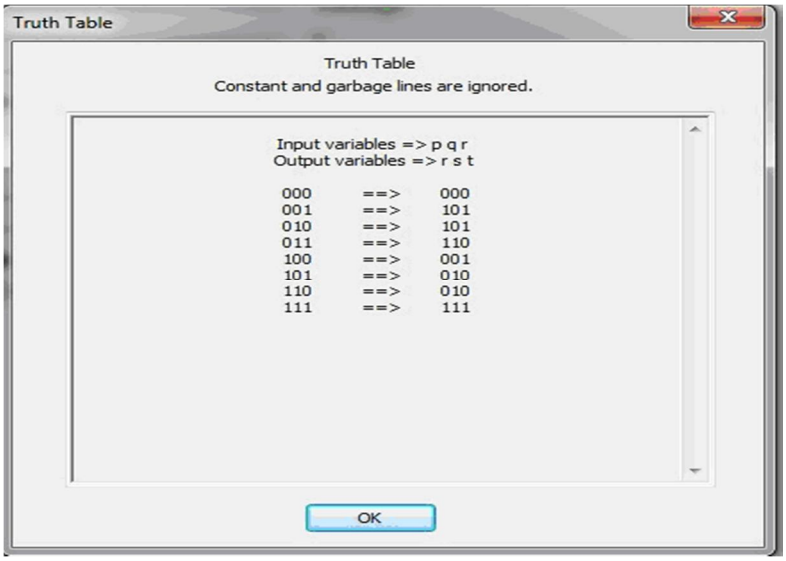


Fig15 Truth table for proposed Quantum Full Adder- Subtractor Circuit after simulation

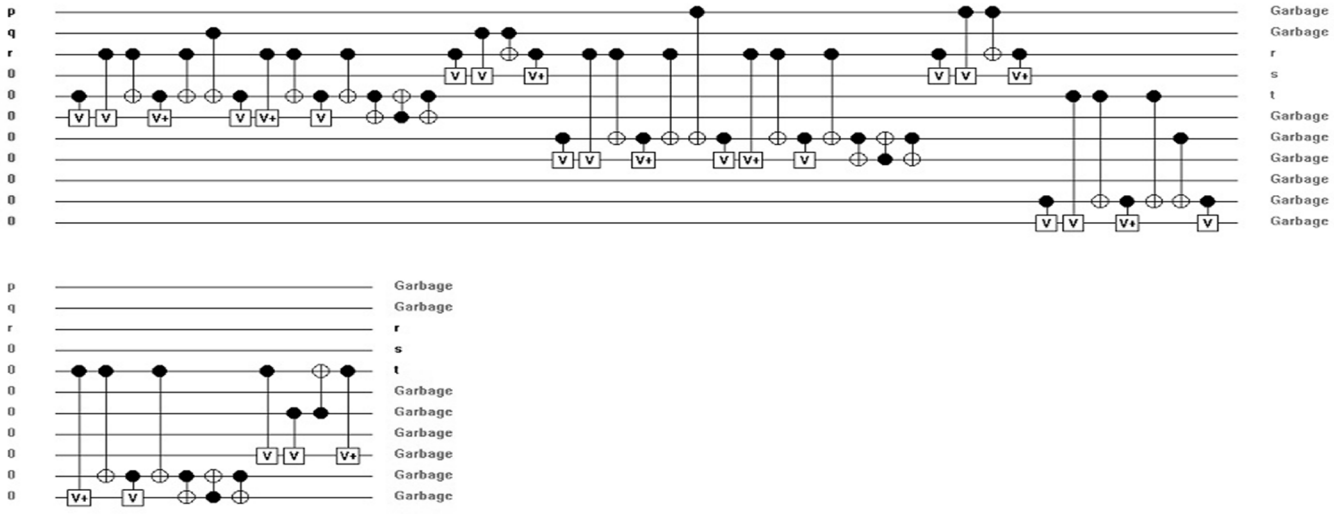


Fig 16 Decomposing proposed circuit with negative control TGs into primitive gate

B. Quantum Cost Calculation

Quantum Cost is the one major performance issue of the quantum circuit. The quantum cost of a circuit is the sum of the quantum costs of its gates. In this paper the quantum realization cost of NOT, CNOT, PERES and Toffoli, swap gate are considered 1, 1, 4, 5

and5 respectively [12].The Quantum cost for Toffoli gate with negative control is 3. According to previously discussed [15] work, quantum cost of a quantum circuit of Islam gate with negative control TG is 18 and gate count is 5 (Fig 9).According to this concept in Fig 14, if we want to calculate the quantum cost for Proposed Full Adder-Subtractor with negative control TGs (quantum cost=3) ,the cost will be 54 and total gate count will be 15,result shown in Fig 18.

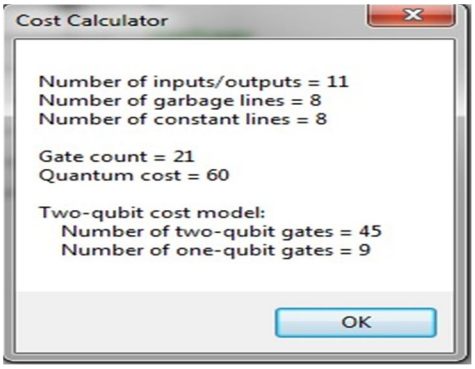


Fig17 Quantum cost of proposed quantum circuit of Full Adder-Subtractor using 3IGs (with +ve control TG)

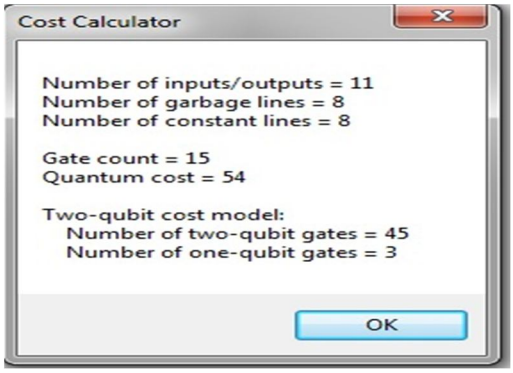


Fig18 Quantum cost of proposed quantum circuit of Full Adder-Subtractor using 3IGs (with -ve control TG)

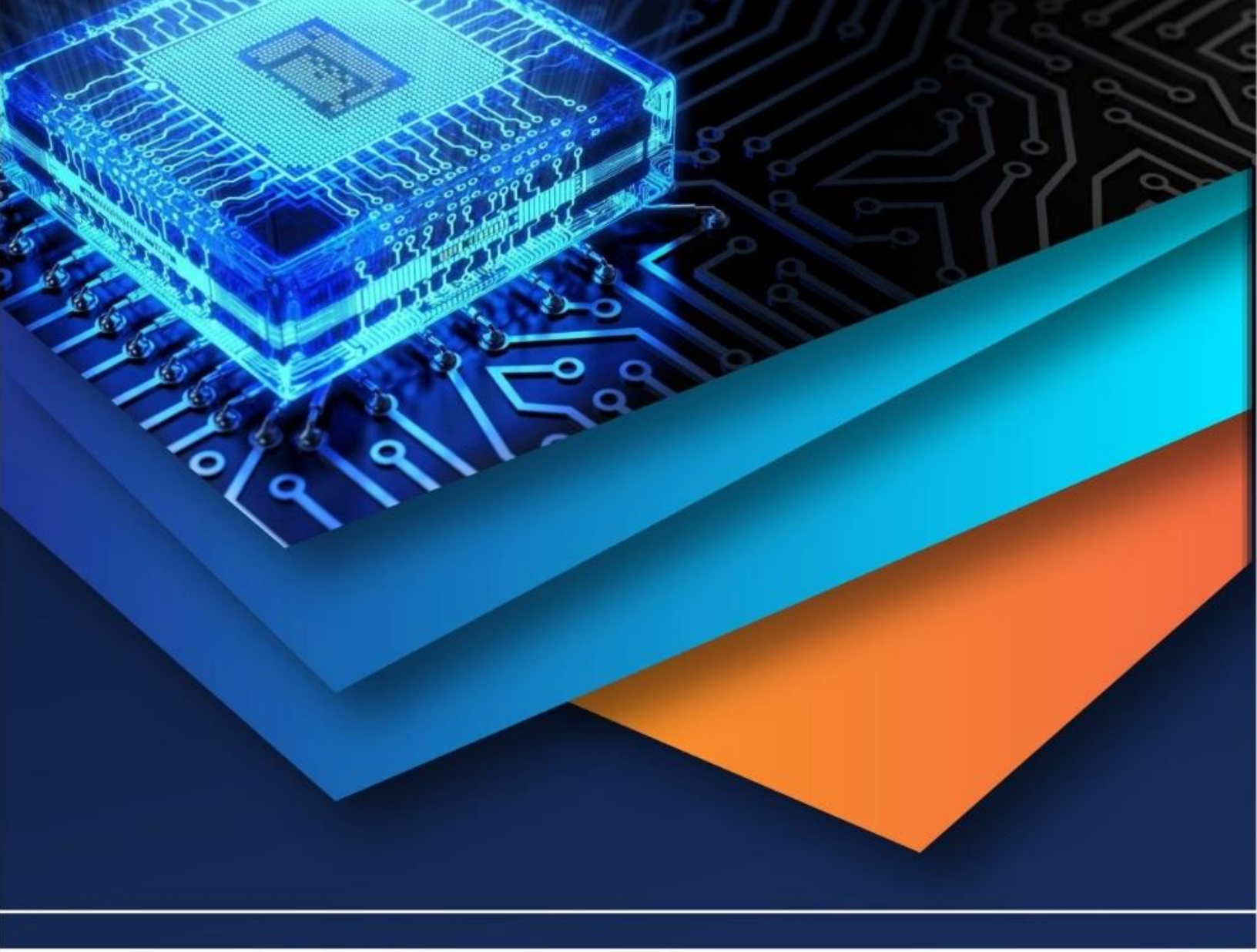
V. CONCLUSIONS

In this paper, proposed Quantum Representation of Full Adder-Subtractor circuit is introduced by 3 quantum realization of Islam Gate Circuits [15]. We find out the general quantum cost from proposed Quantum Circuit. In Future we will try to reduce the quantum cost of this proposed circuit and also find out an overall circuit Probabilistic transfer matrices from gate matrices for evaluates the circuit reliability.

REFERENCES

[1] Moore, Gordon E. (1965). "Cramming more components onto integrated circuits" (PDF). Electronics Magazine. p. 4. Retrieved 2006-11-11.
[2] "Excerpts from A Conversation with Gordon Moore: Moore's Law" (PDF). Intel Corporation. 2005. p. 1. Retrieved 2006-05-02.
[3] Rolf Landauer: "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development, vol. 5, pp. 183-191, 1961.
[4] C. H. Bennett, "Logical Reversibility of Computation," IBM J. Research and Development, Vol. 17, pp. 525-532, November 1973.
[5] Saiful Islam, Muhammad Mahbubur Rahman, Zerina Begum, "Realization of a Novel Fault Tolerant Reversible Full Adder Circuit in Nanotechnology" The International Arab Journal of Information Technology, Vol. 7, No. 3, pp.317-323,July 2010
[6] Smita Krishnaswamy , George F. Viamontes , Igor L. Markov , John P. Hayes ," Accurate Reliability Evaluation and Enhancement Via Probabilistic Transfer Matrices", Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE'05),IEEE Computer Society
[7] Md. Mazder Rahman, Anindita Banerjee_, Gerhard W. Dueck, and Anirban Pathak_," Two-Qubit Quantum Gates to Reduce the Quantum Cost of Reversible Circuit, 2011 41st IEEE International Symposium on Multiple-Valued Logic,pp.86-92,IEEE Computer Society.
[8] William N. N. Hung, Xiaoyu Song, Guowu Yang, Jin Yang, and Marek Perkowski," Quantum Logic Synthesis by Symbolic Reachability Analysis" DAC 2004, June 7–11, 2004, San Diego, California, USA. Pp. 838-841
[9] Mozammel H. A. Khan " Cost Reduction in Nearest Neighbour Based Synthesis of Quantum Boolean Circuits" Engineering Letters, 16:1, EL_16_1_01
[10] Ketan N. Patel, Igor L. Markov and John P. Hayes " Evaluating Circuit Reliability Under Probabilistic Gate-Level Fault Models"
[11] Md. Saiful Islam, Member, IACSIT, Mohd. Zulfiquar Hafiz, and Zerina Begum "Quantum Cost Efficient Reversible BCD Adder for Nanotechnology Based Systems" July 6, 2011
[12] Himanshu Thapliyal, Nagarajan Ranganathan "A New Reversible Design of BCD Adder" 978-3-9810801-7-9/DATE11/©2011 EDAA
[13] http://www.cse.umich.edu/~imarkov/pubs/misc/iwls03-errProb.pdf

[14] http://qcad.sourceforge.jp/
[15] Madhumita Mazumder,Sourav Samanta "Quantum Realization of Islam Gate and Full adder Circuit Design", Micro 2014,Vol.I,1st International Conference on Microelectronices,circuits & Systems, July 11th 2014,ISBN:81-85824-46-0
[16] V.Kamalakannan1, Shilpakala.V2, Ravi.H.N "Design of adder/ subtractor circuits based on reversible gates"IJAREEIE, Vol. 2, Issue 8, August 2013
[17] Theresal T, Sathish K, Aswinkumar R"A New Design of optical Reversible adder and subtractor using MZI"International Journal of Scientific and Research Publications, Volume 5, Issue 4, April 2015 ISSN:2250-31



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY