iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VI **Month of publication:** June 2017

DOI:

www.ijraset.com

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Volume 5 Issue VI, June 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Design and Analysis of 12T MTCMOS and Memristor MCAM using VLSI

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Abstract: ***Memories Are An Integral Part Of Most of the digital devices and hence reducing power consumption of memories as well as area reduction is very important as of today to improve system performance, efficiency and reliability. A transistorized SRAM cell is conventionally used as the memory cell. Large-capacity content addressable memory (CAM) is a key element in a wide variety of applications. The memristor behaves as a switch, much like a transistor. However, unlike the transistor, it is a two-terminal rather than a three-terminal device and does not require power to retain either of its two states. Note that a memristor change its resistance between two values and this is achieved via the movement of mobile ionic charge within an oxide layer, furthermore, these resistive states are non-volatile.***

This project focuses on new approach towards the design and modeling of memristor based CAM (MCAM) using a combination of MOS devices to form a core of a memory or logic cell that forms the building block of the CAM architecture and 6T SRAM and 12T MTCMOS SRAM cell. The non volatile characteristics and the nano-scaled geometry together with compatibility of the memristor with CMOS processing technology increases the packing density, provides for the new approaches towards power management through disabling CAM blocks without loss of stored data, reduces power dissipation, and has scope for speed improvement as the technology matures.

Our proposed work will be, new memory model have been determined and compared with existing models and proposed cell design dissipates less power at different temperatures than existing models. Simulation did on the basis of Microwind 3.1 Back End CMOS Technology to reduce power consumption and enhance data stability.

Keywords— SRAM, MCAM, MTCMOS, BSIM 4, NVRAM, SAR

I. INTRODUCTION

CMOS has become the technology use in many applications in recent years; it is fundamental concept of nMOS logic provide a strong basis both for the conceptual understanding and development of CMOS design. VLSI technology is used in both analog system as well as digital integrated system. This technology has various advantages such as it requires small size of chip, low power consumption, high performance speed, large storage capacity etc. However, such technology needs a complex method to implement on hardware as this technology uses very small size of chips ranging from micro to nanometer of size. It is required to use simulation based circuit design. In addition to transistor-level circuit design issues, the accurate prediction and reduction of interconnect parasitic has become a very significant topic in high-performance digital integrated circuits. In today's day to day life, there is need of storing devices, where these devices require memory to store the data. This term memory is usually refers to the actual chips capable of holding data. DRAM, SRAM, PROM, MCAM, FLASH etc. are types of memory having various properties. Out of which, we explore concept, design and modeling of memory cell as a part of Memristor based Content Addressable Memory architecture using a combination of switch having some fixed resistance value as memristor and n-type MOS devices and SRAM . Memristor predicted by Chua in 1971 and generalized by Kang. Chua invented that new circuit elements defined by the single valued relationship dø=Mdq must exist; whereby current moving through memristor is proportional to the flux of magnetic field that flows through the material and static random access memory the term refers to read and write memory; that is, you can both write and read data into or from RAM .It is volatile, which means that it requires a steady flow of electricity to maintain its contents, It has various advantages such as data does not need to be refreshed dynamically ,able to support faster read and write times etc. To aware customers to choose the best storing device in between different SRAM and MCAM cell with consideration of all parameters? Hence this reason motivated me to select this project. The main objective of this work deals with the design and analysis of high speed performance addressable memory for future search engines to develop low power consumption and no loss of store data in a cell even if the power supply is turn OFF and perform analysis of different transistorized memory cell on the basis of different parameters and power dissipation on different frequency range have been determined for proposed memory model using Microwind 3.5 Back End CMOS technology.

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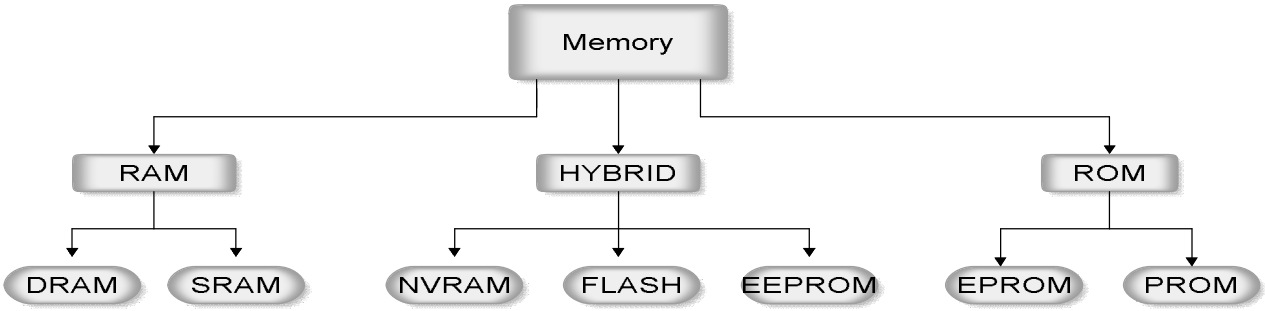

Fig.1.1; Memory Hierarchy

II. LITERATURE SURVEY

From the review of published literature, it is observed that many researchers have designed and analyse various memories by undertaken different systems, processes or phenomena and techniques attempted to find the unknown parameters using VLSI technology.

Circuit theorist Leon Chua introduced memristor as a missing non-linear passive two terminal electric component relating electric charge and magnetic flux linkage [1]. Leon Chua more recently argued that the definition should be generalized to cover all 2-terminal non-volatile memory devices based resistance switching effects. In this paper they explore conceptualization, design, and modeling of the memory cell as part of a memristor-based content addressable memory (MCAM) architecture using a combination of memristor and n-type MOS devices. A typical content addressable memory (CAM) cell forms a SRAM cell that has two n-type and two p-type MOS transistors, which requires both GND connections as well as well-plugs within each cell. Chua postulated that a new circuit element defined by the single-valued relationship must exist, whereby current moving through the memristor is proportional to the flux of the magnetic field that flows through the material. The memristor behaves as a switch, much like a transistor but it has two-terminal device. Note that a memristor changes its resistance between two values and this is achieved via the movement of mobile ionic charge within an oxide layer, furthermore, these resistive states are non-volatile. This behavior is an important property that influences the architecture of CAM systems, where the power supply of CAM blocks can be disabled without loss of stored data. Therefore, memristor-based CAM cells have the potential for significant saving in power dissipation.

Budhaditya Majumdar, Sumana Basu proposed their technique, the SRAM cell operates by charging /discharging of a single bit-line (BL) during read and writes operation, resulting in reduction of dynamic power consumption to that of a conventional 6T SRAM cell [2]. The power consumption is further decreased if the switching operational voltage of the bit-line lies between 0.25VDD to 0.5VDD. All simulations are done using0.18um Technology. Memories are an integral part of most of the digital devices and hence reducing power consumption of memories as well as area reduction is very important issue to improve system performance, efficiency and reliability. This paper presents a novel CMOS 6-transistor SRAM cell for different purposes including low power embedded SRAM applications and stand-alone SRAM applications. The data is retained by the cell with the help of leakage current and positive feedback, and does not use any refresh cycle. Also, the proposed cells uses a single bit-line for both read and write purposes. The cell proposed in this paper consumes less dynamic power and has higher read stability than the standard one. In conventional six-transistor (6T) SRAM cell, read stability is very low due to the voltage division between the access and driver transistors during read operation.

Hong Zhu & V. Kursun proposed their concept eight-transistor SRAM cells that employ separated read and write ports offer stronger data stability as compared to the conventional other cells [3]. The 7T, 8T, 9T, and conventional 6T SRAM cell structures are quantitatively compared. The layouts of the full memory arrays including memory cells and all the peripheral circuitry are drawn with the TSMC 65 nmmulti- CMOS technology. Nine important performance metrics (layout area,data stability, write voltage margin, read speed, write speed, read power consumption, write power consumption, leakage currents, and minimum power supply voltage) are simultaneously considered for a fair and comprehensive benchmarking of the circuits. Memory cells that are immune to parameter variations are desirable in state of the art integrated circuits.

P. Upadhyay, Sarthak Ghosh, R. Kar, D. Mandal, S. P. Ghoshal, has preposed structure two voltage sources are used, one connected with the Bit line and the other one connected with the Bit bar line in order to reduce the swing voltage at the output nodes of the bit and the bit bar lines [4]. Reduction in swing voltage causes the reduction in dynamic power dissipation during switching activity. Because of MTCMOS technology, the SRAM cell is having low VT (LVT) transistors and there are two high VT (HVT)

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sleep transistors as well. Sleep transistors and a LVT Transmission gate (TG) in conjunction are used for reducing the wake up power during transition from sleep mode to active mode and vice versa for writing operations of the SRAM cell. This reduces the static power dissipation of the SRAM cell. Simulation results of static and dynamic power dissipations and power delay product of the proposed SRAM cell have been determined and compared to those of some other exiting models of SRAM cell. Simulation has been done in 45nm CMOS environment with the help of Microwind 3.1. In this paper, a novel 12T MTCMOS based SRAM cell is proposed. A charge recycling technique is used to minimize the power consumption during the mode transition and two voltage sources are used at the output nodes to reduce the swing voltages during switching activity.

By scaling down the technology, we can optimize the parameters like power consumption. Hence considering the advancement of future technology and the advantage of 32 nm technology over 45, 65 and 90 nm technology, the proposed project has been decided to do with the selection of higher order of 32 nm technology.

III. PROBLEM IDENTIFICATION

In the recent years, the VLSI industry is at peak of production. While dealing with the advancement in the technology, various issues are getting involved in the designs. Below 45 nm technology, the transistor becomes leaky and thus the power consumption increases. This case becomes worst at the operating the design for multiple range of frequencies. As we know that the design consumes power at the change in frequency. Thus we have to take care of the change of frequency. Conventional memory cells are not very much compatible with the power versus frequency variations. So, we are going to design the cell that will compatible in a linear manner with change in frequency and trying to find out cell stability. Memory processing has been considered as the pace-setter for scaling a technology. A number of performance parameters including capacity (that relate to area utilization), cost, speed, area, active power consumption, standby power, robustness such as reliability and temperature related issues characterize memories. We are trying to achieve better performance parameters of 32nm based memory structures such as MCAM, MTCMOS and SRAM cell and also trying to solve the main problem of SRAM, MTCMOS and CAM cell is that they cannot store the data when the power supply is turned OFF by using MCAM cell.

IV. METHODOLOGY

The flow chart of the proposed methodology is shown in figure 3.1.

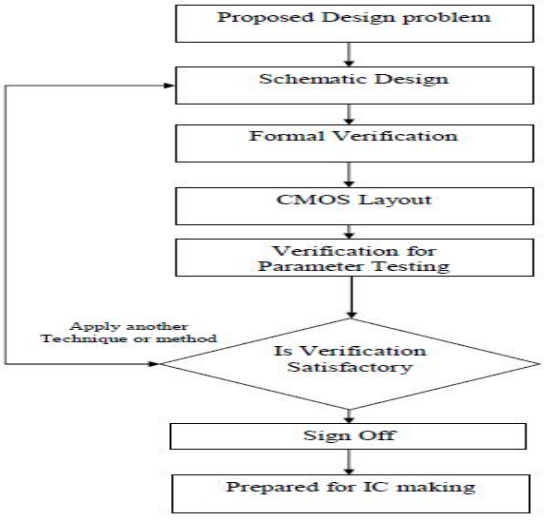

Fig.4.6. Design Flow Chart

A. To achieve the proposed target fallowing steps are include in the design and analysis of proposed phase-locked loop.

1) Schematic design of proposed SAR logic based ADC using CMOS transistors (BSIM4).

2) Performance verification of the above for different parameters.

3) CMOS layout for the proposed all types of oscillators using VLSI backend.

4) Verification of CMOS layout and parameter testing.

5) If the goal is achieved for all proposed parameter including detail verification, sign off for the design analysis and design will be ready for IC making.

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6) If detail verification of parameters would not completed then again follow the first step with different methodology.

B. A key circuit use in modern communication, processors and in many systems is oscillator. The oscillators are use is to create a periodic logic or analog signal with a stable and predictable frequency. In today's communication system, processors and computing devices require circuit of low power consumption, small size, high speed & low fabrication cost. Here we are going to design the oscillator that solves the problem of power consumption, area consumption and generate the desired frequency band

1) Work Flow Through

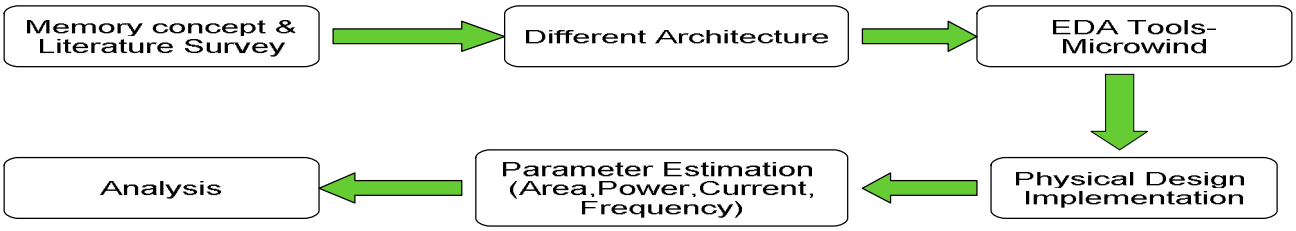

Fig.3.2.1 (a) Work Flow Through

The block diagram shown in fig.3.2.1 consists of Work flow of the project design. It is related with different block which explain below:

a) Memory Concept & Literature Survey: First block relates with actual meaning of memory and review of published literature, it is observed that many researchers have designed various memories by applying different techniques with consideration of different parameters.

b) Different Architectures: Consist of design of different architectures of memory models which is taken into consideration.

c) EDA Tool-Microwind: We will use MICROWIND software allows us to simulate and design an integrated circuit at physical description level. This package contains a library common logic and analog ICs to view and simulate the various design to obtain different parameters. We can gain access to circuit simulation by pressing one single key. The electric extraction of circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

d) Physical design implementation: The gate material has long been polysilicon (SiO2) as the insulat or between the gate and the channel. The atom is a convenient measuring stick for this insulating material beneath the gate, commonly known as gate oxide. In 32 nm technology, the high K dialectic is used. It enables the thinner equivalent oxide thickness while keeping the leakage current low. While dealing with physical design implementation, here in the project, we will follow the Lambda based design rules.

2) CMOS layout design rules

The purposes of the design rules are to guarantee the precise layout according to the rules defined by the specific process. The rules are the worst process deviation: mask misalignment, over etching etc. More layers will need more layout design rules. The typical 13-layer CMOS 1.8um EPROM design rules and programs are described below. They can be easily modified for SRAM, DRAM or other technologies.

a) Minimum width: In order to prevent the line layer from notching or necking, the minimum width for each specific layer is defined; such as minimum width for active, polyl, poly2, or metal layers.

b) Minimum spacing:

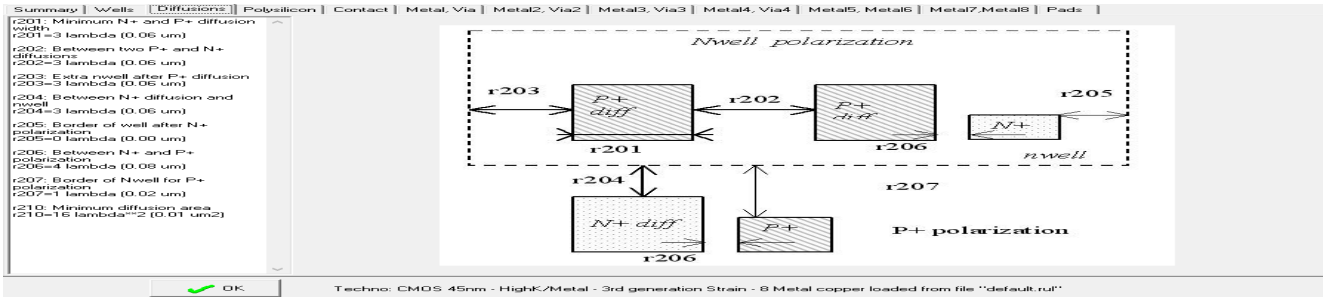

Fig.3.2.1 (b) Design rules

The line to line spacing is defined to avoid line shorts or bridging for polyl, poly2 and metal layers. Also, the minimum active spacing is usually specified to prevent active to active leakage in punch through mode.

c) *Overlap:* This check is for two overlapped layers. Normally it is needed to check metal contact, poly contact or active contacts. For different voltages, different overlap rules are required.

d) *Misalignment:* Misalignment between masking layers 19 determines design rules. There are two kinds of alignments. 1) Direct alignment 2) Indirect alignment. In this process, n-well is a major flat layer, active and p-field to n-well are direct alignments, active to p-field is an indirect alignment, polyl, poly2, N+ implant and P+ implant to active are direct alignments. They are in indirect alignments with each other. Contact to poly2, metal to contact and pad to metal are direct alignments.

3) CMOS colormap and technology files

In general, colormap and technology files are needed only for layout drawing. To create a layout drawing, we need to specify all the layers. "A technology file defines various masks and symbolic layers in a cell. This file also defines the color, fill pattern, and outline pattern used to display each layer, and references a colormap file that sets each layer's color^^.

a) *Parameter estimation:* Once the physical design implemented, we need to think about two types of optimization in CMOS design as:In logical optimization, we need to optimize the design trends in the form of logic. But once the logic is done, we need to take care of physical design optimization. Here we need to improve the placement of the design. We need to improve the physical area of the design and the most important factor a power of the design. That we are going to achieve with the current design trend.We have find out and improved various design parameters such as area, power, current and effect of change in frequency on the power.

b) *Analysis:* In the analysis part, we are doing certain case studies on the power. We are checking the effect of change in frequencies on the operating power of the design implemented. Also we are performing various parametric analysis on the design as effect of change in capacitance on the power, change in temp and effect on the design working and so on.

V. CONCLUSION

The proposed Memory will design using 32nm CMOS/VLSI technology with Microwind 3.5 EDA tool. The main novelties related to the 32 nm technology are the high-k gate oxide, metal gate and very low-k interconnect .This Software used in a program allows us to design and simulate an integrated circuit at physical description level. The non-volatile characteristic and nanoscaled geometry of the memristor together with its compatibility with CMOS process technology increases the memory cell packing density, reduces power dissipation and provides for new approaches towards power reduction and management through disabling blocks of MCAM cells without loss of stored data. Here we will estimate and present simulation results by implementing the circuit layouts in32 nm technology. We will try to achieve simulation results pointed out that structures designed and simulated almost eliminate leakage and yielded a reduction in leakage between 45%- 70% depending on the control voltage used and also the parametric analysis simulation will perform on the design in order to get the cell stability by varying the cell input frequency with respect to the change in power. From the analysis of various parameters of SRAM and MCAM CELL, it will be conclude that which cell is most preferable than other memory models.

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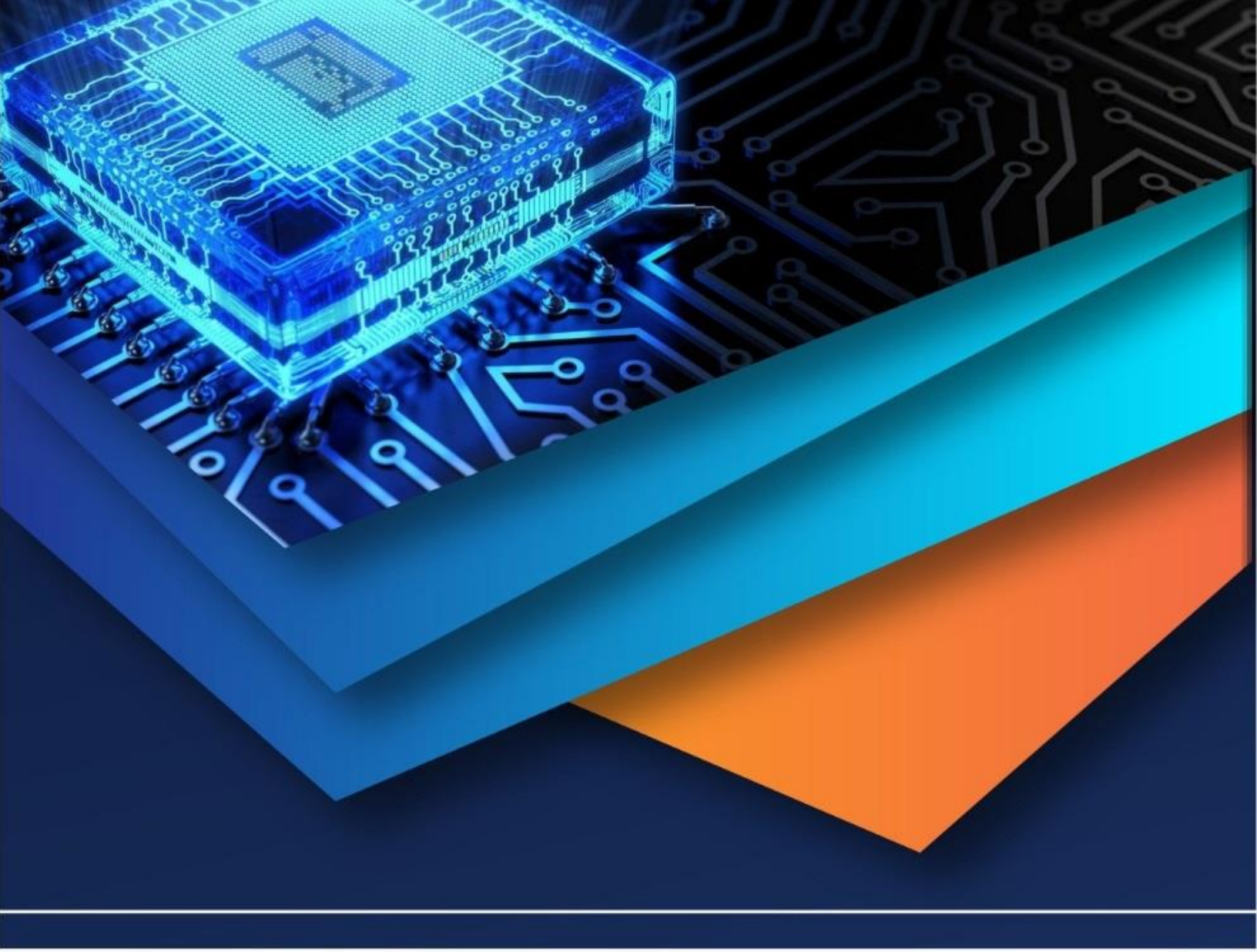

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