



IJRASET

International Journal For Research in
Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 Issue: VII Month of publication: July 2017

DOI:

www.ijraset.com

Call:  08813907089

E-mail ID: ijraset@gmail.com

Design Of Low Power Baugh-Wooley Multiplier

Ku. Shweta N. Yengade¹, Prashant R. Indurkar²

¹M.Tech Student, Department Of Electronics and Telecommunication, B.D.C.O.E, Wardha, Maharashtra, India

²Associate Professor, Department Of Electronics and Telecommunication, B.D.C.O.E, Wardha, Maharashtra, India

Abstract: In VLSI design the performance of any system is determined by the performance of the elements of the system. Multiplier is the slow element in the system. The multiplier speed is depends on multiplication technique and type of adder. This paper proposes the type of architecture of 32 bit Baugh-Wooley multiplier. The code is implemented in XILINX ISE 14.5 software. The delay and power of 32 bit Baugh-Wooley multiplier obtained after synthesis and is compared with existing multiplier and found that the proposed Baugh-Wooley multiplier circuits seems to have better performance in terms of delay and power.

Keywords: VLSI, system, Baugh-Wooley Multiplier, XILINX, etc.

I. INTRODUCTION

Day by day a faster design with smaller area and lower power consumption is essential for the modern electronic designs . In microelectronics design multiplier is a fundamental unit and widely used in circuits, for which the multiplication process should be optimized properly. Multipliers generally have extended latency, huge area and consume substantial amount of power. Hence designing of low-power multiplier has become an important part in VLSI system design.

Multiplication involves two basic operations- the generation of the partial product and their accumulation. Therefore, there are possible ways to speed up the multiplication that reduces the complexity, and as a result reduces the time needed to accumulate the partial products. Both solutions can be applied simultaneously.

A. Baugh-Wooley Two's Complement Signed Multiplier

Two's Compliments is the most popular method in representing signed integers in Computer Sciences. It is also an operation of negation (Converting positive to negative numbers or vice -versa) in computers which represent negative numbers using two's complements. Its use is so wide today because it does not require the addition and subtraction circuitry to examine the signs of the operands to determine whether to add or subtract.

| +N | Positive Integers | -N | Negative Integers | | |
|----|-------------------|----|-------------------|----------------|----------------|
| | | | Sign & Magnitude | 2's Complement | 1's Complement |
| +0 | 0000 | -0 | 1000 | ---- | 1111 |
| +1 | 0001 | -1 | 1001 | 1111 | 1110 |
| +2 | 0010 | -2 | 1010 | 1110 | 1101 |
| +3 | 0011 | -3 | 1011 | 1101 | 1100 |
| +4 | 0100 | -4 | 1100 | 1100 | 1011 |
| +5 | 0101 | -5 | 1101 | 1011 | 1010 |
| +6 | 0110 | -6 | 1110 | 1010 | 1001 |
| +7 | 0111 | -7 | 1111 | 1001 | 1000 |
| +8 | ---- | -8 | ---- | 1000 | ---- |

Fig. 1 a: - Two's complement and One's complement representation

Two's complement and one's complement representations are commonly used since arithmetic units are simpler to design. Fig.1 shows Two's & One's complement representation.

B. Baugh-Wooley Two's complement Signed numbers

Baugh-Wooley Two's complement Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits. Baugh-Wooley technique was developed to design direct multipliers for Two's complement numbers. When multiplying Two's complement numbers directly, each of the partial products to be added is a signed number. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree. According to Baugh-Wooley approach, an efficient method of adding extra entries to the bit matrix suggested to avoid having deal with the negatively weighted bits in the partial product matrix. In fig 1 (b) & (c) partial product arrays of 5*5 bits Unsigned and Signed bits are shown.

| | | | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|-------|
| | | | | a_4 | a_3 | a_2 | a_1 | a_0 | |
| | | | | x_4 | x_3 | x_2 | x_1 | x_0 | |
| | | | | | | | | | |
| | | | | a_4x_0 | a_3x_0 | a_2x_0 | a_1x_0 | a_0x_0 | |
| | | | a_4x_1 | a_3x_1 | a_2x_1 | a_1x_1 | a_0x_1 | | |
| | | a_4x_2 | a_3x_2 | a_2x_2 | a_1x_2 | a_0x_2 | | | |
| | a_4x_3 | a_3x_3 | a_2x_3 | a_1x_3 | a_0x_3 | | | | |
| a_4x_4 | a_3x_4 | a_2x_4 | a_1x_4 | a_0x_4 | | | | | |
| | | | | | | | | | |
| P_9 | P_8 | P_7 | P_6 | P_5 | P_4 | P_3 | P_2 | P_1 | P_0 |

Fig. 1 b: - 55 Unsigned multiplication

| | | | | | | | | | |
|----------|-----------|-----------|-----------|-----------|----------|----------|----------|----------|-------|
| | | | | a_4 | a_3 | a_2 | a_1 | a_0 | |
| | | | | x_4 | x_3 | x_2 | x_1 | x_0 | |
| | | | | | | | | | |
| | | | | $-a_4x_0$ | a_3x_0 | a_2x_0 | a_1x_0 | a_0x_0 | |
| | | | $-a_4x_1$ | a_3x_1 | a_2x_1 | a_1x_1 | a_0x_1 | | |
| | | $-a_4x_2$ | a_3x_2 | a_2x_2 | a_1x_2 | a_0x_2 | | | |
| | $-a_4x_3$ | a_3x_3 | a_2x_3 | a_1x_3 | a_0x_3 | | | | |
| a_4x_4 | $-a_3x_4$ | $-a_2x_4$ | $-a_1x_4$ | $-a_0x_4$ | | | | | |
| | | | | | | | | | |
| P_9 | P_8 | P_7 | P_6 | P_5 | P_4 | P_3 | P_2 | P_1 | P_0 |

Fig. 1 c: - Signed multiplication

Figure 1 (c) shows how this algorithm works in the case of a 5x5 multiplication. The first three rows are referred to as PM (partial products with magnitude part) and generated by one NAND and three AND operations. The fourth row is called as PS (partial products with sign bit) and generated by one AND and three NAND operations with a sign (with magnitude part) and generated by one NAND and three AND operations. Consider the partial products of PM. Suppose $b_2 = b_0$ in figure 1 (c). Then the third row can be obtained by shifting the first row by 2 bits. Likewise, shift operation can be used to obtain a partial product of different bit level as in sign magnitude multiplication. Baugh-Wooley schemes become an area consuming when operands are greater than or equal to 32 bits. The rest of the paper is organised as follows. The Baugh-Wooley architecture is explained in section 2. Implementation results in terms of power, area, and speed 4 bit multipliers and comparison are presented.

C. Baugh-Wooley Architecture

Hardware architecture for Baugh-Wooley multiplier is shown in fig 2. It follows left shift algorithm. Through MUX (multiplexer) we can select which bit will multiply. Suppose we are adding +5 and -5 in decimal we get '0'. Now, represent these numbers in 2's complement form, and then we get +5 as 0101 and -5 as 1011. On adding these two numbers we get 10000. Discard carry, then the number is represented as '0'.

| | | | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|-------|
| | | | | a_4 | a_3 | a_2 | a_1 | a_0 | |
| | | | | x_4 | x_3 | x_2 | x_1 | x_0 | |
| | | | | | | | | | |
| | | | | a_4x_0 | a_3x_0 | a_2x_0 | a_1x_0 | a_0x_0 | |
| | | | a_4x_1 | a_3x_1 | a_2x_1 | a_1x_1 | a_0x_1 | | |
| | | a_4x_2 | a_3x_2 | a_2x_2 | a_1x_2 | a_0x_2 | | | |
| | a_4x_3 | a_3x_3 | a_2x_3 | a_1x_3 | a_0x_3 | | | | |
| a_4x_4 | a_3x_4 | a_2x_4 | a_1x_4 | a_0x_4 | | | | | |
| | | | | | | | | | |
| P_9 | P_8 | P_7 | P_6 | P_5 | P_4 | P_3 | P_2 | P_1 | P_0 |

Fig. 1 d :- 5*5 Multiplication example of Baugh-Wooley architecture

D. Baugh-Wooley Multiplier

Baugh- Wooley Multiplier is used for both unsigned and signed number multiplication. Signed Number operands which are represented in 2's complemented form. Partial Products are adjusted such that negative sign move to last step, which in turn maximize the regularity of the multiplication array. Baugh- Wooley Multiplier operates on signed operands with 2's complement representation to make sure that the signs of all partial products are positive. Here are using fewer steps and also lesser adders. Here a_0, a_1, a_2, a_3 & b_0, b_1, b_2, b_3 are the inputs. The outputs are p_0, p_1, \dots, p_7 . Pipelining register used in this architecture, so it will take less time to multiply large number of 2's complement but less than 32 bit. Above 32 bit Modified Baugh-Wooley Multipliers used.

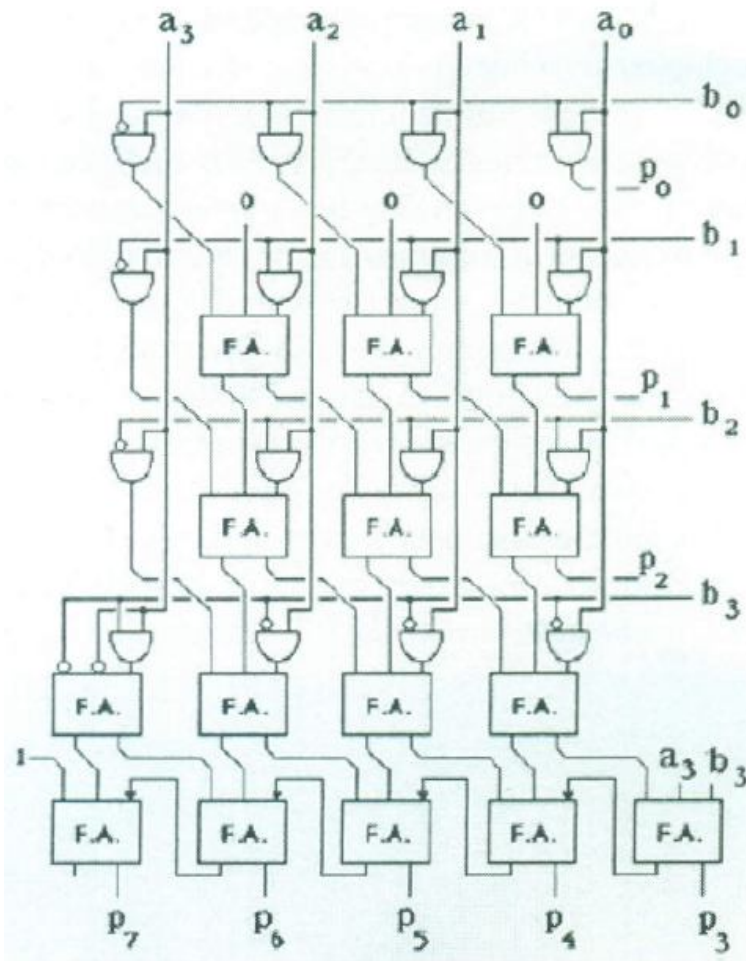


Fig. 2:- Block diagram of 4*4 Baugh-Wooley multiplier

II. IMPLEMENTATION ON XILINX SOFTWARE

Now we are moving towards main programming parts. Using the Baugh-Wooley multiplier we have to develop a program. In this paper the 32 bit multiplier is designed in VHDL (very high speed integrated circuits hardware description language). Synthesis and simulation was done in XILINX ISE 14.5. project navigator and simulator integrated in the XILINX package. XILINX is software which is purely based on the VHDL language. VHDL is Very Large Scale Integrated Circuit Hardware Description Language. We have performed our programming using the Vertex6XC6VCX75T FF84-2. Integrated Software Environment is a software tool produced by Xilinx for synthesis and analysis of HDL design, enabling the developer to synthesize their design, perform time analysis, examine RTL diagrams, simulate a design reaction to different stimuli, and configure the target device with the programmer. It includes ISE simulator which we can use for functionality verification of program.

III. EXPERIMENTAL RESULT

The result of the 32 bit Baugh-Wooley multiplier is given in the figures below in which 32-bit number is in binary form. Also the RTL schematic of Baugh-Wooley multiplier is given

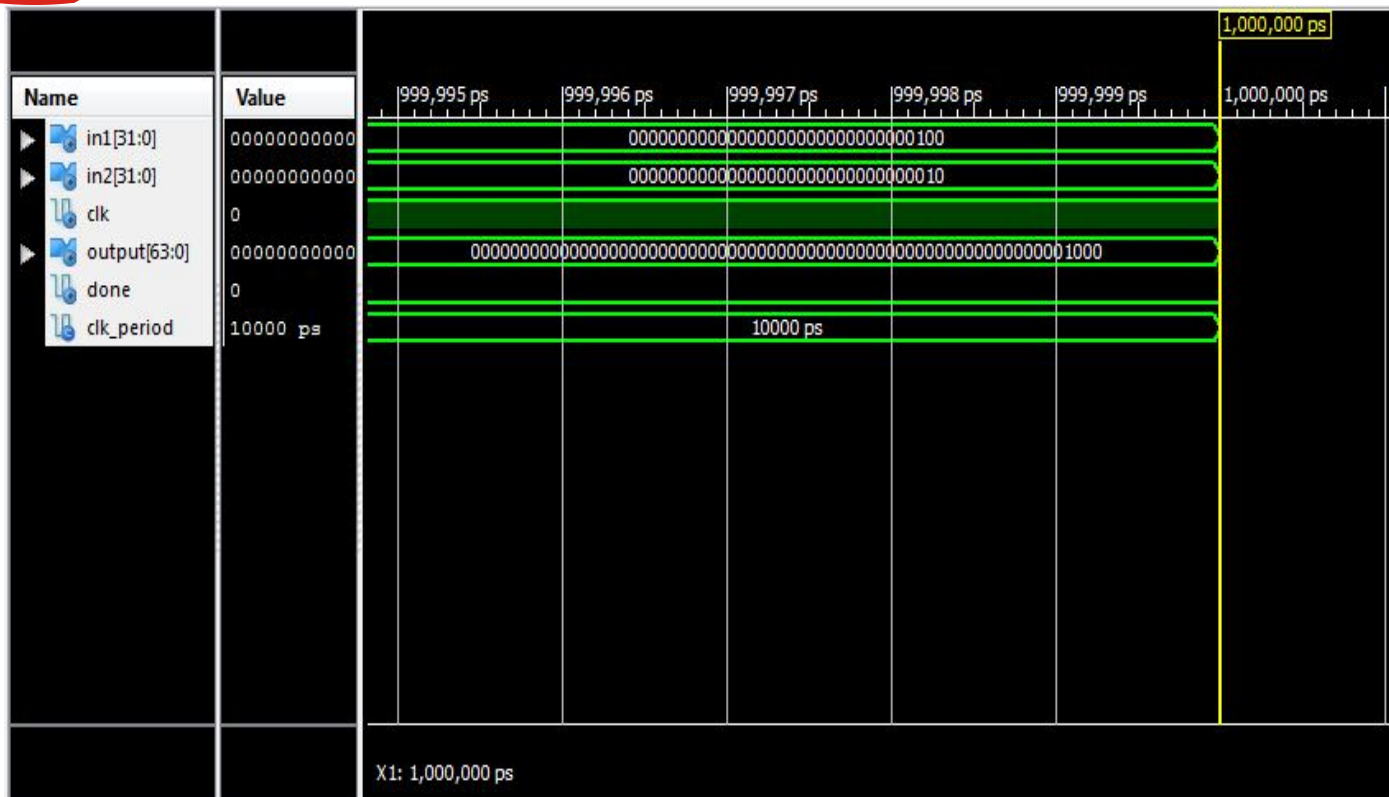


Fig. 3 – Simulation result of Baugh-Wooley Multiplier

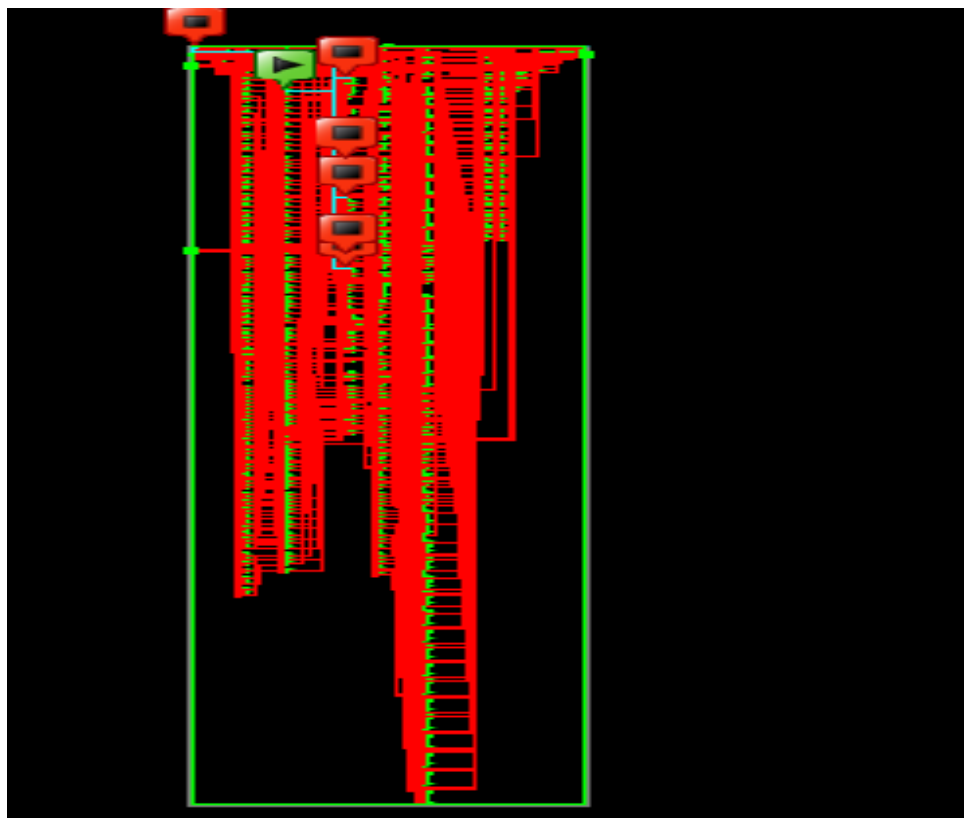


Fig. 4- RTL view of Baugh-Wooley Multiplier

Table 1 –Result of device utilization of Baugh-Wooley Multiplier

| REF PAPER | NAME OF MULTIPLIER | DELAY(n s) | POWER(m W) | NO. OF SLICE LUT'S | DEVICE /FAMILY |
|-----------------|--------------------|------------|------------|--------------------|---------------------------|
| Proposed Design | Baugh-Wooley | 3.584 | 0.0012 | 738 | Virtex 6 XC6VCX75T FF84-2 |

Table 2- comparison of existing method with proposed method

| REF PAPER | NAME OF MULTIPLIER | DELAY(n s) | POWER(m W) | DEVICE /FAMILY |
|-----------------|--------------------|------------|------------|---------------------------|
| [12] | Baugh-Wooley | 6.496 | - | - |
| [5] | Booth | 3.68 | 9.74 | - |
| Proposed Design | Baugh-Wooley | 3.584 | 0.0012 | Virtex 6 XC6VCX75T FF84-2 |

From this table we conclude that power required for Baugh-Wooley multiplier is less than other existing multiplier.

IV. ACKNOWLEDGMENT

We would like to thanks Mr. P. R. Indurkar, Associate Professor, Electronics and telecommunication department, B.D.C.O.E. for his valuable suggestion. We would thanks to our college for providing facilities which help us in our work. We also express thanks to our parents, friends and colleagues.

V. CONCLUSION

The proposed Baugh-Wooley multiplier is simulated using XILINX ISE 14.5. The comparison between proposed and existing multiplier is shown in table 2. From that table we conclude that Baugh-Wooley multiplier have less power than existing multiplier.

REFERENCES

- [1] Maraju SaiKumar, D.Ashok Kumar,Dr.P.Samundiswary, "Design and Performance Analysis Of Multiply-Accumulate(MAC) Unit,"2014 International Conference on Circuit,Power and Computing Technologies [ICCPCT]
- [2] Thirumala Rao V. , Girish Gandhi S. & Leela Mohan C, "Performance Evaluation of Parallel Multipliers for High Speed MAC Design,"International Journal of Innovations in Engineering and Technology(IJiet).
- [3] P.A. Irfan Khan & Ravi Shankar Mishra, "Comparative Aanalysis of different algorithm for design of High-Speed multiplier Accumulator Unit(MAC) ,"Indian Journal of science and technology,Vol 9(8),DOI:10.17485/ijst/2016/v9i8/83614, February 2016.
- [4] Kandimalla Rajaneesh & M.Bharathi, " A Novel High performance Implementation of 64 Bit MAC Units and Their Delay Comparison,"International Journal of Engineering Research and Applications,ISSN:2248-9622,Vol.4,Issue 6(Version6),June2014,pp.122-127
- [5] Magnus Sjalandar & Per Larsson-Edefors , "High –Speed and Low –Power Multipliers Using The Baugh-Wooley Algorithm And HPM Reduction Tree,"October 2008,DOI:10.1109/ICECS.2008.4674784,Source:IEEE Xplore
- [6] Rakesh Warriar, C.H.Vun & Wei Zhang, "A Low-power Pipelined MAC Architecture using Baugh-Wooley based multipiler,"2014 IEEE 3rd global conference on consumer electronics(GCCE)
- [7] Tung Thanh Hoang,Magnus Sjalander, and Per Larsson-Edefors, "High-Speed ,Energy –Efficient 2-Cycle Multiply-Accumulate Architecture,"978-1-4244-4941-5/09/\$25.0015©2009 IEEE
- [8] R.Sakthivel, K. Sravanthi,and H. M.Kittur,"Low power energy efficient MAC,"in ACCI.ACM,2012.
- [9] K.Kalaiselvi and H.Mangalam, "Area Efficient High Speed and Low Power MAC unit", International Journal of computer Application(0975-8887) Volume 67-No 23, April 2013
- [10] P.Jagadeesh,Mr.S.Ravi, and Dr kittur Harish Mallokarjun, "Design of High Performance 64 Bit MAC Unit",ICCPCT-2013
- [11] Promodini Mohonty, "An efficient Baugh-Wooley architecture for signed and unsigned fast multiplication", NIET Journal of Engineering & Technology, Vol. 1, Issue 2, 2013
- [12] Rakesh Kumar, Pradeep Kumar, "An Efficient Baugh-Wooley Multiplication Algorithm for 32-bit Synchronous Multiplication" , International Journal of Advanced Engineering Research and Science (IJAERS) , [Vol-1, Issue-2, July 2014] ISSN: 2349-649



10.22214/IJRASET



45.98



IMPACT FACTOR:
7.129



IMPACT FACTOR:
7.429



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089  (24*7 Support on Whatsapp)