iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VII **Month of publication:** July 2017

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor:6.887
Volume 5 Issue VII, July 2017- Available at www.ijraset.com

Design and Performance Analysis of Two Stage OPAMP Under Impact Of Scaling

Pardeep[1], Ajay Kumar[2]
[1,2] *Department of Electronics and Communication Engineering, GJUS&T (Hisar)*

Abstract: ***In this paper two stage CMOS operational amplifier has been designed and the effect of aspect ratio has been analysed on various characteristics of operational amplifier. The op-amp operates at 2.5V power supply. Various parameters such as Gain, Phase Margin, Common mode Gain, Common mode rejection ratio, Slew Rate are measured and compared for different channel widths of the CMOS. With the decrease in channel width there is a reduction in Gain, Common mode rejection ratio, Slew Rate, Settling time, Rise time whereas the phase margin shows a steep positive change. The designed operational amplifier exhibits a gain of 68.57dB with a 99.55^0 phase margin. Mentor graphics Pyrix schematic tool has been used for the design and simulation.***
Keywords: ***Two stage, CMOS, Operational amplifier, Stability, Phase Margin, Gain, Slew rate, Scaling.***

I. INTRODUCTION

The electronics industry has shown an exploded growth over the last few decades. Majority of the electronic devices in today's world are manufactured using CMOS technology. Operational Amplifier is one of the basic building blocks of most of the electronics devices, ranging from movable electronics to telecommunications and transportation [1]. With each generation of CMOS technologies, the design of op-amps continues to pose a challenge as the supply voltage and transistor channel length scale down [2]. Nowadays the design of analog Circuits such as operational amplifiers in CMOS technology has become more critical [3]. High gain in operational amplifiers is not the only desired parameter instead simultaneously optimizing all parameters has become mandatory. There is a trade-off among power, speed, gain and other performance parameters at different aspect ratio.

Operational amplifiers with high gains and reasonable gain bandwidth product are usually implemented with two-stage structures [4]. A high-gain and stable two- stage CMOS operational amplifier has been designed. The variation in the performance of the op-amp with variations in the width of the CMOS is discussed. Mentor Graphics Pyrix Schematic tool has been used for design and simulation of Two-stage op-amp.

II. BLOCK DIAGRAM OF TWO STAGE CMOS OP-AMP

The Op-amp consists of mainly four functional blocks. Differential amplifier is the first block. Inverting and non-inverting terminals are the two input terminal of differential amplifier. The general block diagram of an op-amp is shown in figure 1.

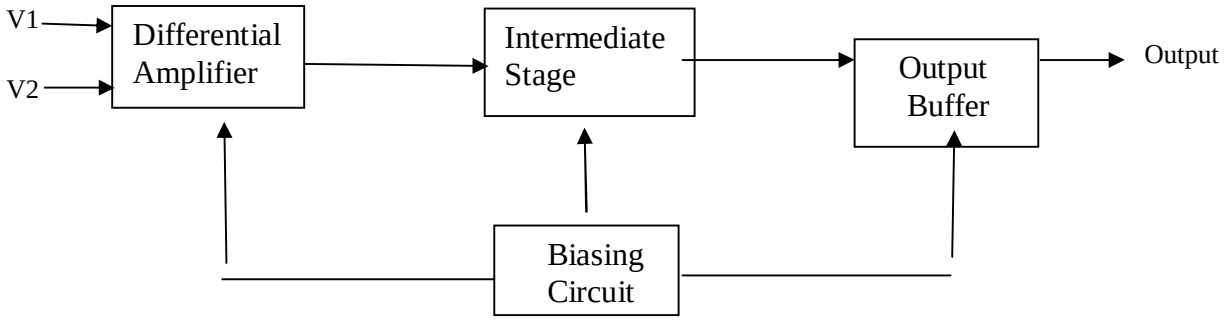


Figure 1. Block diagram of Op-Amp

Intermediate stage uses differential input unbalanced output differential amplifier, to provide extra required gain. The transistors operate in saturation region and the operating point for transistors is provided by the bias circuit. The last block is output buffer stage which provides the low output impedance and larger output current needed to improve the slew rate of the operational amplifier. Many integrated applications do not need low output impedance so the output stage can be dropped. The compensation circuit is used to reduce the gain at high frequencies and to maintain stability when negative feedback is applied to the op amp.

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor:6.887
Volume 5 Issue VII, July 2017- Available at www.ijraset.com

III. DESIGN OF THE OP-AMP

The two-stage op amp is designed with an n-channel input pair [5]. It consists of a total of 9 transistors. Transistor M2, M6, M5, M8 forms the differential amplifier. The inverting input is provided to gate of M8 and non-inverting input is provided to gate of M5.The inverting and non-inverting inputs are denoted by Vn and Vp. The Current mirror circuit formed by transistor M2, M7 and DC current source, is used to bias the operational amplifier. A biasing circuit [6] has been used which provides high dynamic current when the differential input voltages are applied. A DC current of 18µA magnitude is used to bias the operational amplifier. Transistor M3 and M9 are acting as an inverter and helps in increasing the overall gain of the op-amp. A positive capacitive feedback compensation technique [7] which has negligible effect on the stability, is used to increase the slew rate of the operational amplifier. The magnitude of feedback capacitor is 3picofared. The reference value of channel length is L=1.4µm. The reference width of transistors used is given in the table 1. The designed circuit of two stage operational amplifier is as shown below in figure 2.

Channel width values for operational amplifier. Table 1

Transistor	**Width (µm)**
M1, M6	12
M5, M8	12
M4	4
M2,M7	20
M3,M9	90

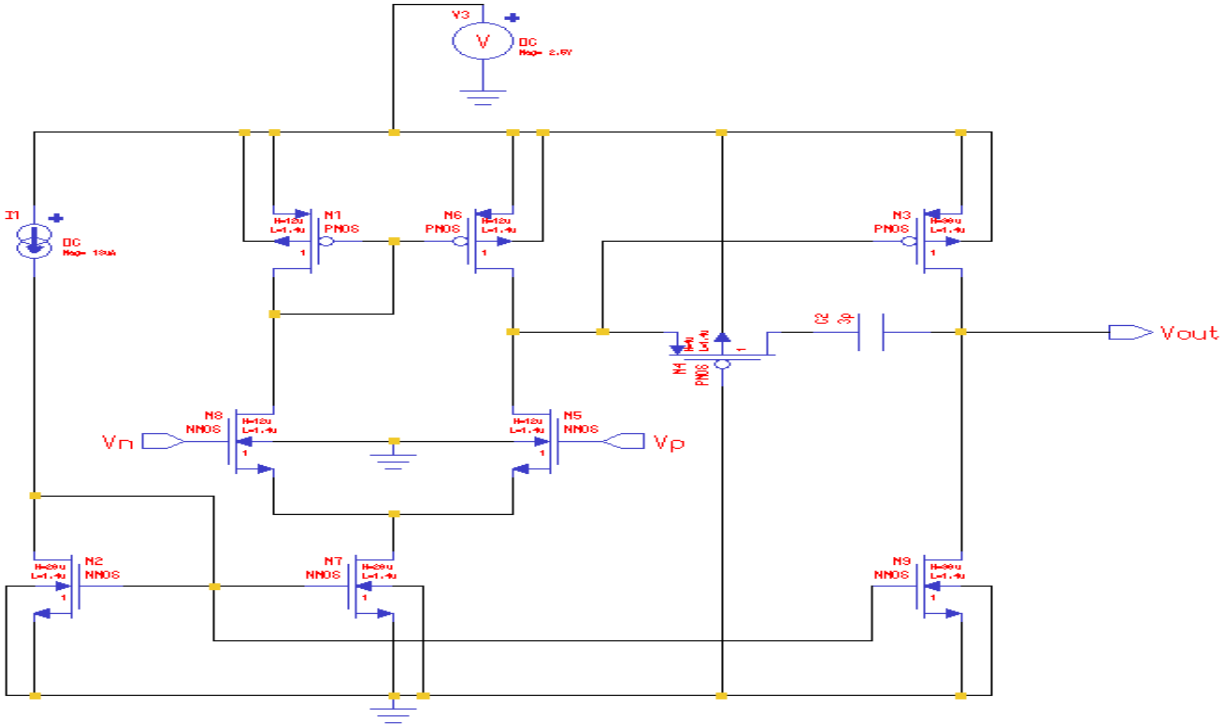


Figure 2. Schematic design of 2 stage CMOS Op-Amp [5]

IV. SIMULATION RESULTS

The simulation results of various parameters for channel length of L=1.4µm are given below

A. Open Loop Gain

The ratio between output voltage and differential input voltage is known as open loop gain As shown in Figure 3, the open loop gain is measured as 68.18 dB

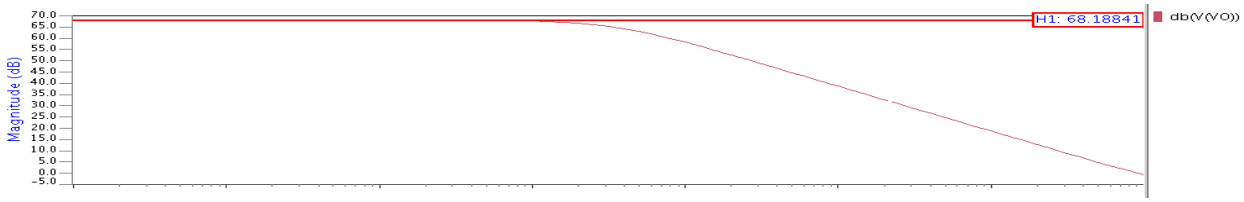


Figure 3. Open loop gain measurement

B. Phase Margin

Phase margin is used to easure the phase with which output differs from the input. It is a measure of the stability of the system. The system is unstable for negative or zero value of phase margin. The system is stable for positive value of phase margin. The value of phase margin measured for the designed circuit is shown in figure 4 and is found to be 99.55degree.

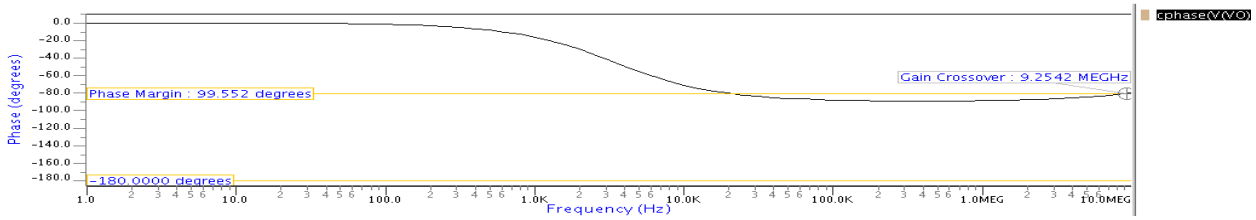


Figure 4. Phase margin measurement

C. Common Mode Gain

Common mode gain is the gain of the differential amplifier with same signal at both the terminals. The measured common mode gain is -13.985 db and is shown in figure 5

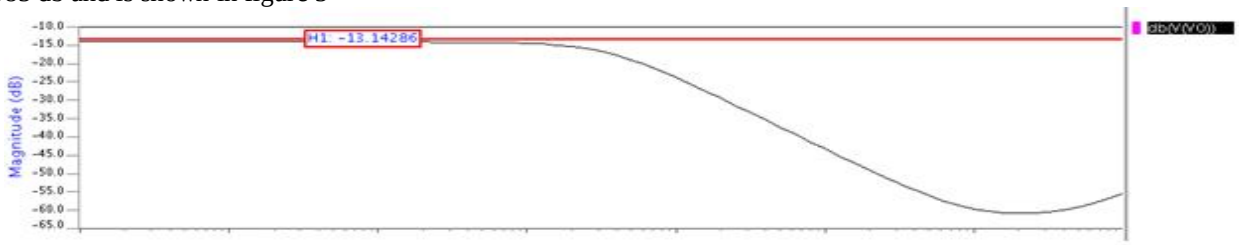


Figure 5. Common mode gain measurement

D. Slew Rate

It is a measure of maximum rate of change of output voltage with respect to time (dvo/dt). It has unit of v/µsec and is found to be 4.0055 v/µsec.

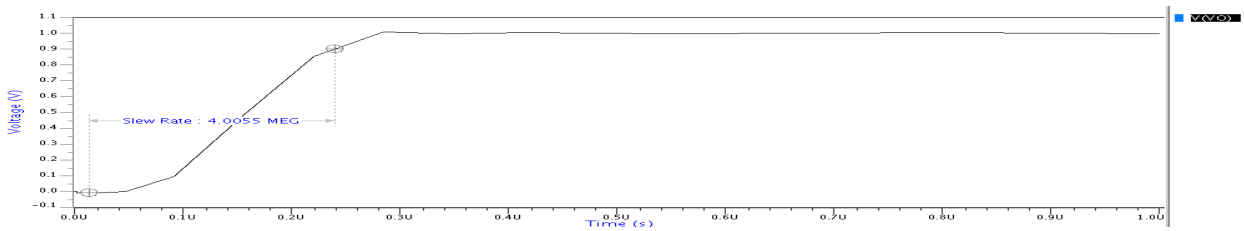


Figure 6. Slew Rate measurement

E. Settling Time

The settling time of an amplifier is the time at which the transient response of the system dies out. As shown in the figure 7 its measured value is 261.49 nsec.

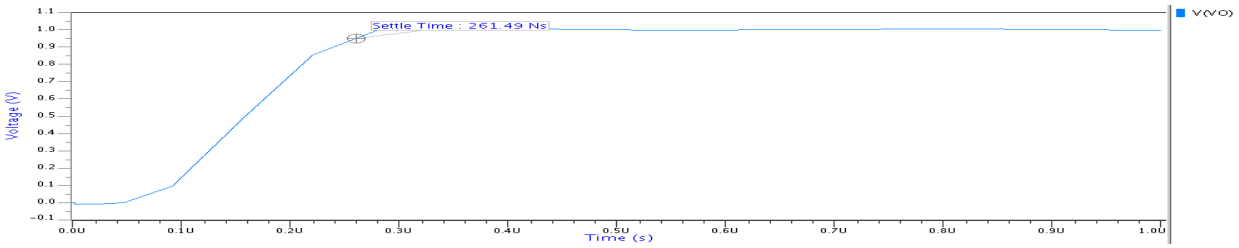


Figure 7. Settling time measurement

F. Rise Time

It is the time required by the output to go from10% to 90% of its final value. It is measured to be 226.59 nsec as shown in figure 8.

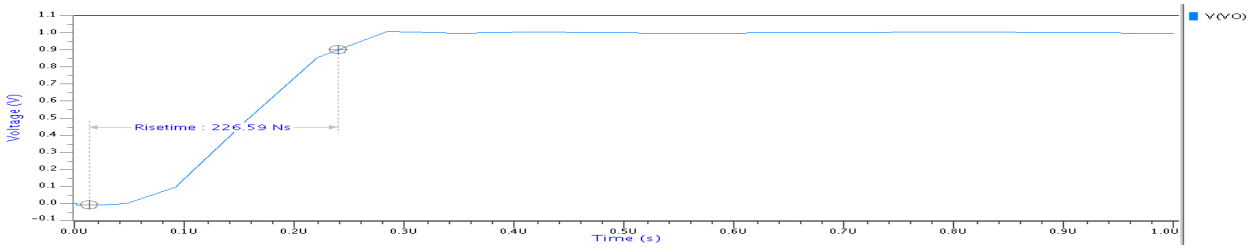


Figure 8. Rise time measurement

G. Common Mode Rejection Ratio

It is the ability of a device to remove the noise signal from the desired signal. It is the ratio of differential gain to common mode gain. To measure it in db the addition of common mode gain with the open loop gain is done. The cmrr for designed circuit is found to be 82.55 db

VI. SCALING

While maintaining the electrical properties of the device, proportional adjustment of the dimensions of an electronic results in a device either larger or smaller than the un-scaled device is called scaling.

A. Impact of Scaling is Characterized in Terms of Following Indicators

1) Feature size
2) Number of gates on IC
3) Power dissipation
4) Operational frequency
5) Production cost

Here we decrease the width of transistors in the reference circuit and determine the various parameters. The result of various parameter after scaling is given in the table 2 as below

Table 2.
Parametric values for different channel widths

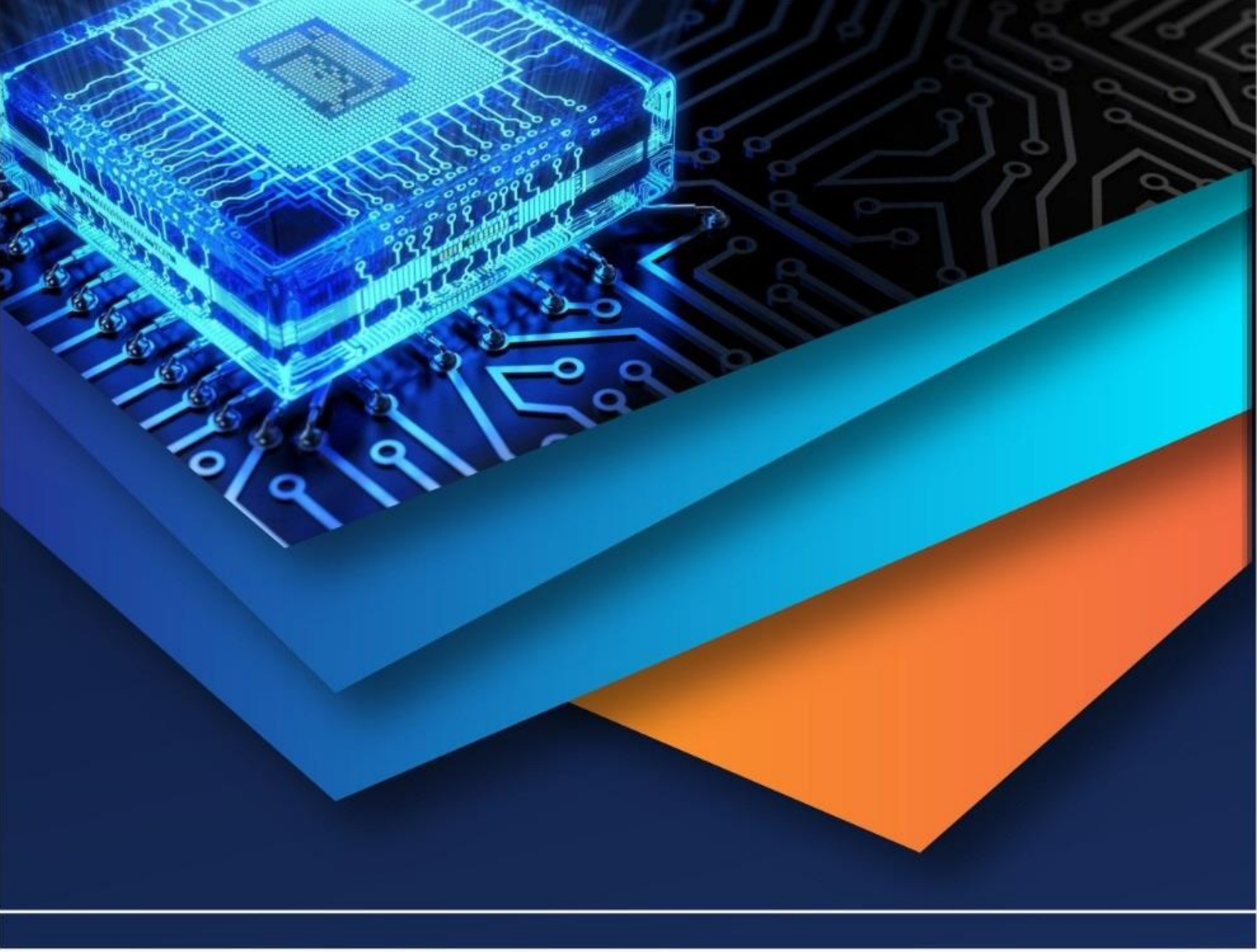
Result	W	W/2	W/3
Gain(dB)	68.18	52.10	46.81
PM(degree)	99.55	120.60	135.07
Common mode gain(dB)	-13.98	-29.29	-33.69
Common mode rejection ratio(dB)	82.55	81.39	80.507
Slew Rate(V/us)	4.0055	3.8918	3.8074
Settling time(ns)	261.49	272.57	283.90
Rise time(nsec)	226.59	233.85	239.93

VII. CONCLUSION

This paper presented the design of a two stage CMOS Op-Amp and analyses its behaviour for various channel widths. Tables of different parameters for various Channel widths is drawn which shows that as the width of the transistor channel decreases, all measured parameters except phase margin decreases. It is observed that the stability of the designed op-amp increases as phase margin increases with decrease in channel width; at the cost of reduced gain and slow response

REFERENCES

[1] H. Iwai, Extended Abstracts 2008 ,"8th International Workshop on Junction Technology (IWJT '08)," Shanghai Shanghai,China 2008 May 15-16, IEEE Press) p. 1. [DOI:10.1109/IWJT.2008.4540004].
[2] Sanjeev Gupta, "Electronics Devices and Circuits," Dhanpat Rai Publication, 2008.
[3] Maria del Mar Herschensohn, Stephen P. Boyd, Thomas H. Lee, "GPCAD: A Tool for CMOS Op-Amp Synthesis" International Conference on Computer-Aided Design, November 1998.
[4] Hamed Aminzadeh and Reza Lotfi, "Design guidelines for high-speed two stage CMOS Operational Amplifiers", The Arabian Journal for Science and Engineering, Volume 32, Number 2C, pp.75-87, December 2007.
[5] Amana Yadav, " Design of Two-Stage CMOS Op-Amp and Analyze the Effect of Scaling" ©Ijaet Issn: 2248-9622, Vol. 2, Issue 5,September-October 2012, Pp.647-654
[6] Soumy Ranjan Ghosh, Kamran Khan "A Low Power Adaptive Bias fully differential operational amplifier"ISBN No. 978-1-4799-3914-5141$31.00©2014IEEE
[7] Alireza Mesri, Mehmoud Mehdipour Pirbazari " High gain two-stage amplifier with positive capacitive feedback compensation" IET Circuit Devices Syst., 2015, Vol.9, Iss. 3,pp.181-190 doi:10.1049/iet_cds.2014.0139



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY