iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VIII **Month of publication:** August 2017

DOI: http://doi.org/10.22214/ijraset.2017.8150

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor:6.887
Volume 5 Issue VIII, August 2017- Available at www.ijraset.com

Design of 8-Bit and 16-Bit Adder-Subtractor with Optimized Power and Quantum Cost

Prinkle Wadhawan[1], Amandeep Singh Bhandari[2]
[1,2]*Department of ECE, Punjabi University Patiala*

Abstract: Reversible logic gates have gained interest in design of circuits in VLSI due to its low power consumption and one- to-one mapping of input and output bits. The paper represents the design of 8-bit and 16-bit adder-subtractor using various reversible logic gates. The basic AND, OR, NOT gates and the universal NAND, NOR gates are irreversible. Reversible logic gates are superior to irreversible logic gate with respect to parameters such as power consumption, quantum cost, power dissipation etc. In this paper the adder-subtractor circuit has been designed using DKG gate and WG gates. The proposed design has improved the existing circuit in terms of quantum cost and power consumption.
Keywords: Reversible logic gates, quantum cost.

I. INTORDUCTION

The use of irreversible logic gates in circuits lead to energy dissipation into the environment. This energy dissipation is associated with information loss. Laws of physics suggest that KTln2 Joules energy is dissipated for every one bit of information loss, where K is Boltzmann constant and T is absolute temperature [1]. In 1973, C.H. Bennett concluded that ideally the reversible logic gates have zero power dissipation [2]. Further with the increase in device density of the chip, power dissipation becomes a critical problem. As a solution reversible logic gates were developed. The reversible logic is used in a number of real time applications. For a gate to be reversible it must satisfy two conditions. Firstly, its inputs and outputs must be uniquely retrievable from each other (logical reversibility) and secondly, the reversible logic based device should run backwards (physical reversibility).
A reversible logic gate is a logic circuit consisting of equal number of inputs and outputs (say N), making it an N*N gate. Let the input vector be $I_v = I_1, I_2, I_3, \ldots\ldots I_N$ and the output vector be $O_v = O_1, O_2, O_3, \ldots\ldots O_N$, then an N*N reversible logic gate can be shown as:

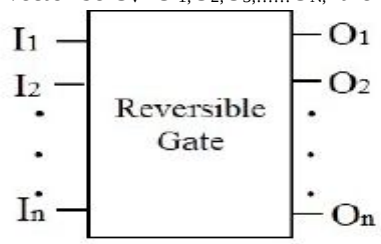

Fig. 1 N*N Reversible logic gate symbol [10]

A. There are several parameters for deciding the quality and performance of the circuits.
1) *Number of Reversible Gates (N):* The amount of reversible gates employed in the circuit.
2) *Number of Constant Inputs (CI):* This refers to the amount of inputs that are to be maintained constant at either zero or one so as to synthesize the given logical function [7].
3) *Number of Garbage Outputs (GO):* This refers to the amount of unused output in a reversible logic circuit. One cannot avoid the garbage outputs as these are essential to attain reversibility [15].
4) *Quantum Cost (QC):* This refers to the value of the circuit in terms of the value of a primitive gate. It is calculated by knowing the amount of primitive reversible logic gates (1*1 and 2*2) needed to make the circuit [9].

B. There are some conditions for any gate to be reversible that are following [6][12]:
1) Number of inputs and outputs should be same.
2) No feedback and no fan-out is allowed.
3) Minimum number of reversible gates should be used.
4) Minimum number of constant inputs and minimum number of garbage outputs should be produced.

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II. BASIC REVERSIBLE LOGIC GATES

A. Feynman Gate

Feynman gate is a 2*2 reversible gate as shown in figure 2[3]. The input vector is I (A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A⊕B. The quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs. The block diagram of Feynman gate is shown below:

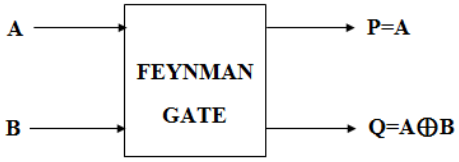


Fig. 2 Feynman Gate [3]

B. Double Feynman Gate

Double Feynman gate is a 3*3 reversible gate as shown in figure 3[4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C. Quantum cost of Double Feynman gate is 2. Its block diagram is shown below:

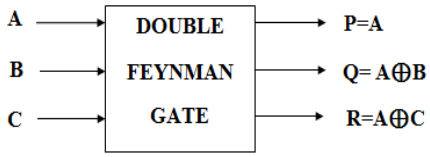


Fig. 3 Double Feynman Gate [4]

C. Toffoli Gate

Toffoli gate is a 3*3 reversible gate as shown in figure 4 [5]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5. Its block diagram is shown below:

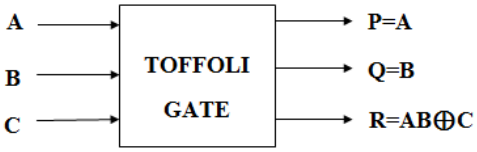


Fig. 4 Toffoli Gate [5]

D. WG Gate

WG gate is a 4*4 reversible logic gate as shown in figure 5. Its input vector is I(A, B, C, D) and the output vector is O(P, Q, R, S). The output of WG gate is P=A, Q=A⊕B⊕D, R=A⊕B⊕C, S= (A⊕D⊕B)(A⊕D⊕C) ⊕(A⊕D). The quantum cost of this gate is 7. Its block diagram is shown below:

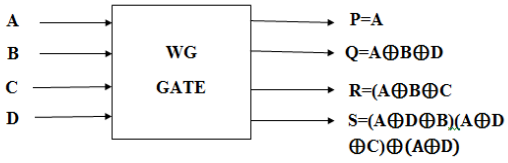


Fig. 5 WG Gate [16]

E. DKG Gate

DKG gate is a 4*4 reversible gate as shown in figure 6[12]. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). The output is defined by P=B, Q=A'C⊕AD', R= (A⊕B) (C⊕D) ⊕CD and S=B⊕C⊕D. Quantum cost of DKG gate is 6. Its block diagram is shown below:

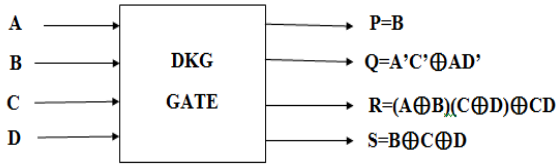


Fig. 6 DKG Gate [11]

III. PROPOSED WORK

A. Design 1: 8-Bit Adder-Subtractor Using DKG Gates

In this approach DKG gates are used for adder Subtractor design. As shown in figure 7, the design has a total of 8 DKG gates cascaded to work as 8-bit adder-subtractor.the Binary numbers A and B are applied to the second and third inputs of DKG gate whereas as first input is connected to mode and fourth input is also connected to mode for first gate whereas for all other gates is connected to previous carry. This design approach generates a total of 16 garbage outputs. Quantum cost of this design is 48. The expression for adder and subtractor is given below [13]:

Sum=A⊕B⊕C_{IN}

Carry= (A⊕B) C_{IN}⊕AB

Difference=A⊕B⊕C_{IN}

Borrow=A'B+BC_{IN}+C_{IN}A'

Where C_{IN} is the previous carry in case of adder and previous borrow in case of subtractor [8].

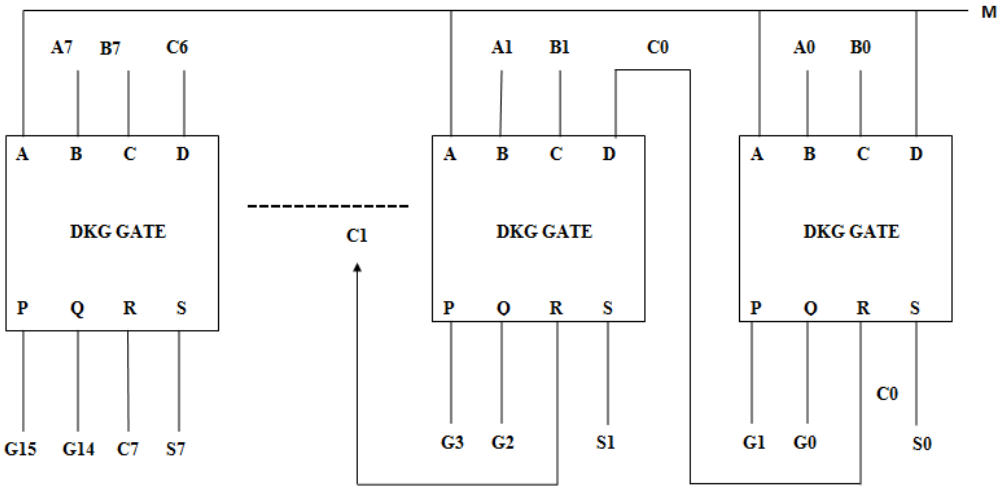


Fig. 7 Proposed design for reversible 8-bit adder-subtractor using DKG gate

B. Design 2: 16-Bit Adder Subtractor using WG Gates

In this design WG gates are used. As shown in figure 8 the design has 16 WG gates are cascaded to function as adder as well as subtractor. Binary inputs A and B are applied to first and second inputs of the WG gate and third input is connected to mode for first gate whereas for all other gates it is connected to previous carry and fourth input will select the mode of operation. Quantum cost of the circuit is 112.

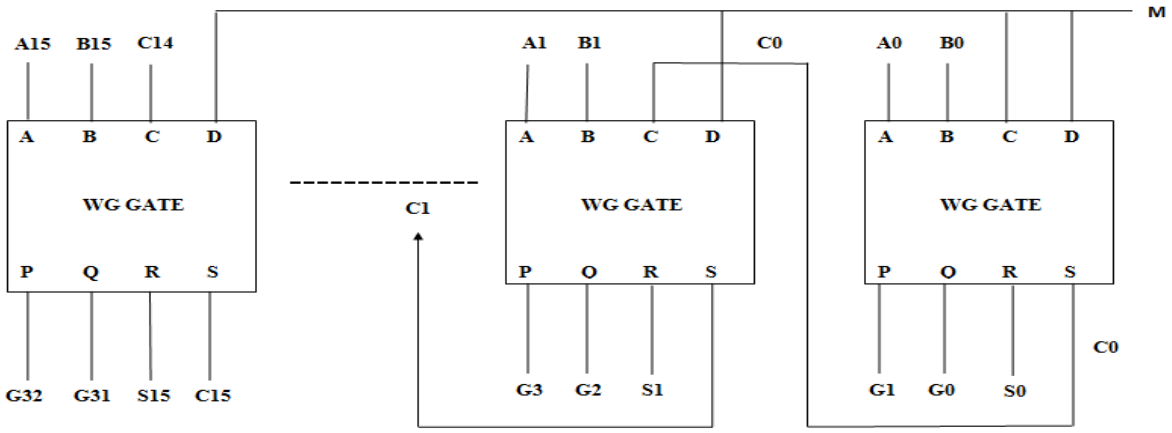


Fig. 8 Proposed design for reversible 16-bit adder-subtractor using WG gate

C. Design 3: 16-Bit Adder Subtractor using DKG Gates

The design has a total of 16 DKG gates cascaded to work as 16-bit adder-subtractor. This design approach generates a total of 32 garbage outputs. Quantum cost of this design is 96.

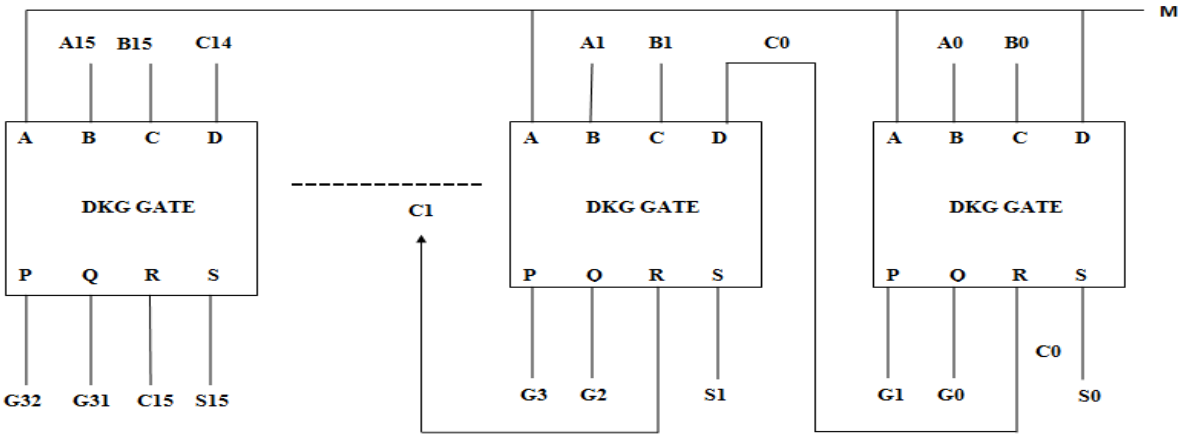


Fig. 9 Proposed design for reversible 16-bit adder-subtractor using DKG gate

IV. IMPLEMENTATION AND RESULTS

A. Design 1

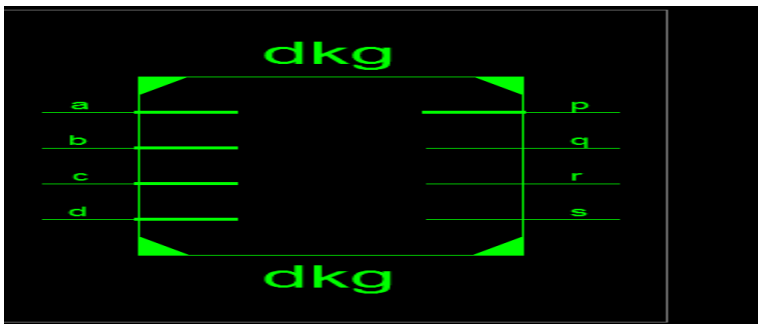


Fig. 10 RTL view of DKG gate

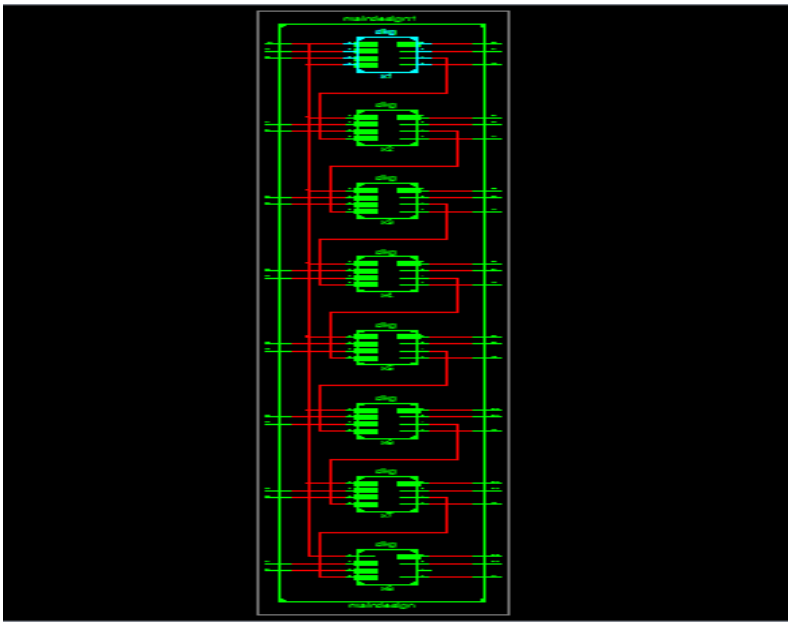


Fig. 11 RTL view of synthesized 8-bit adder-subtractor using DKG gates

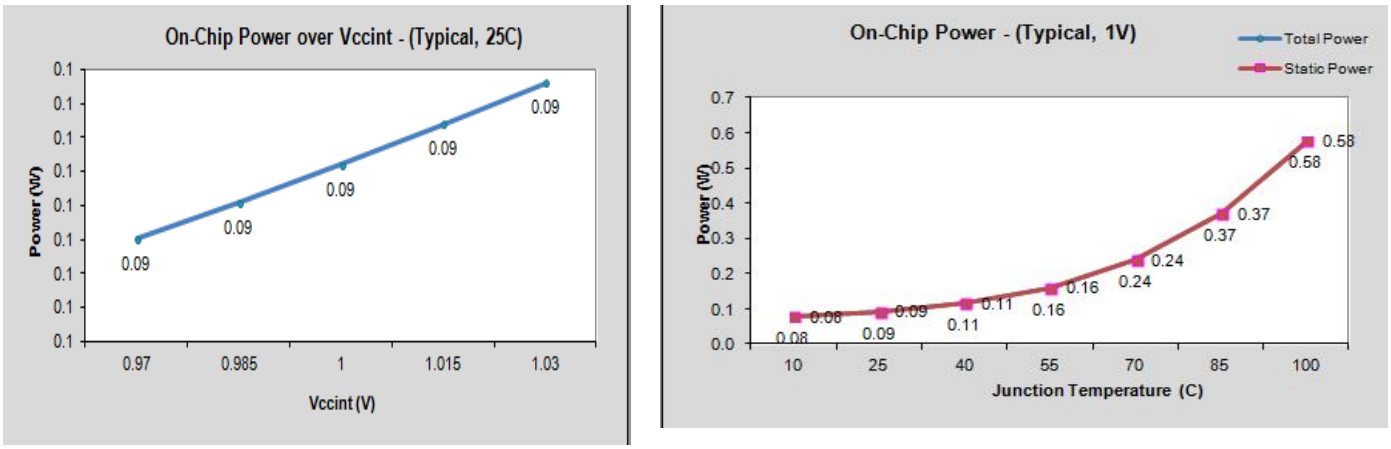


Fig. 12 Power Consumption for reversible 8-bit adder-subtractor using DKG gate

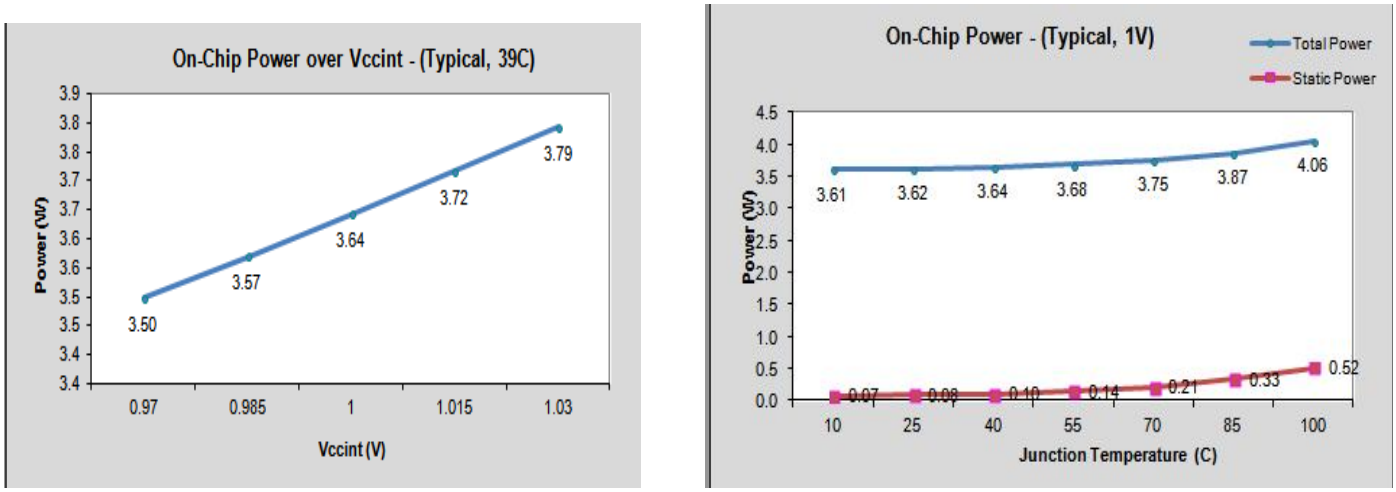


Fig. 13 Power Consumption for existing reversible 8-bit adder-subtractor using WG gate

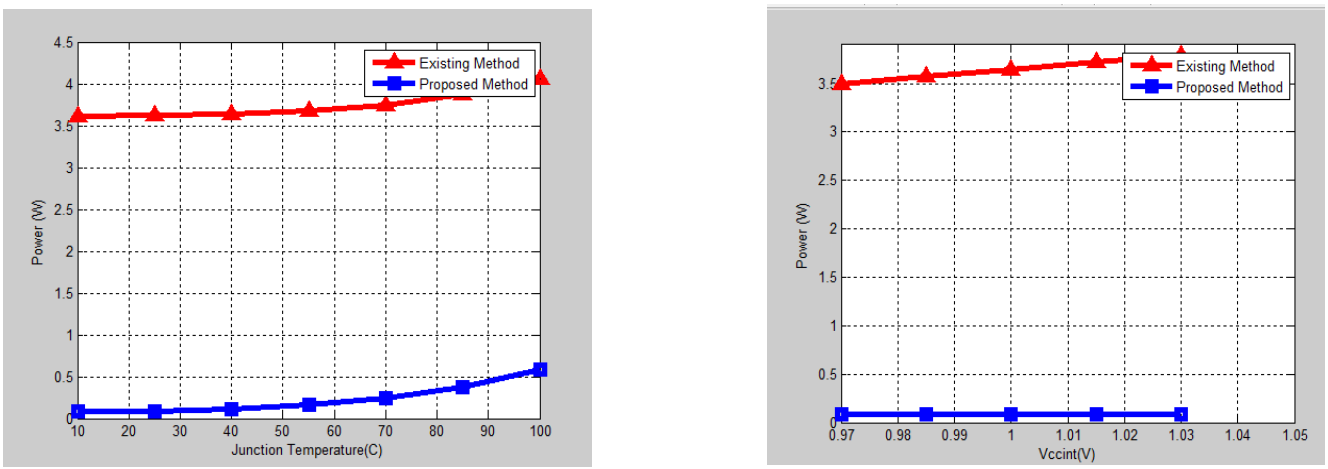


Fig. 14 Comparative results of power consumption graph for proposed and existing design.

B. Design 2

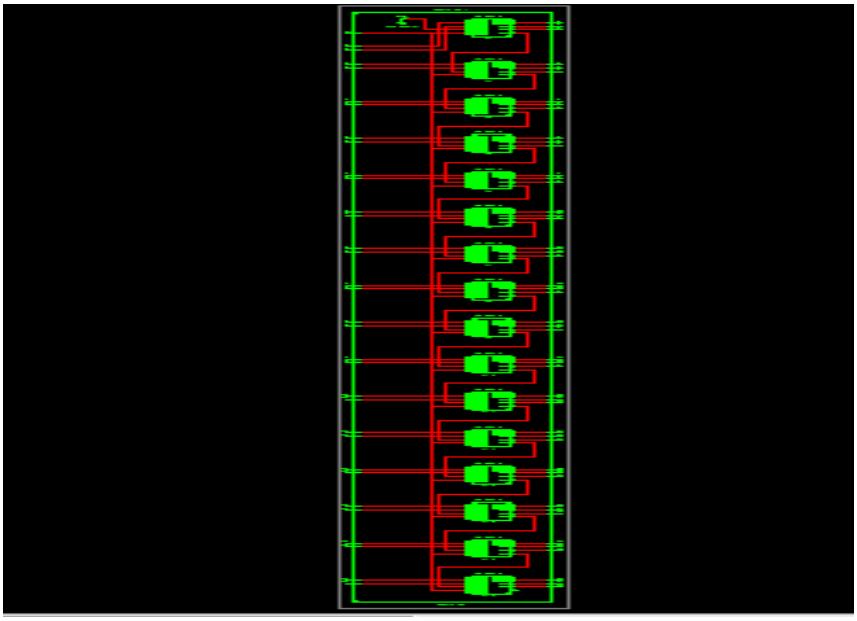


Fig. 15 Proposed design of 16-bit Adder-Subtractor circuit using WG gates

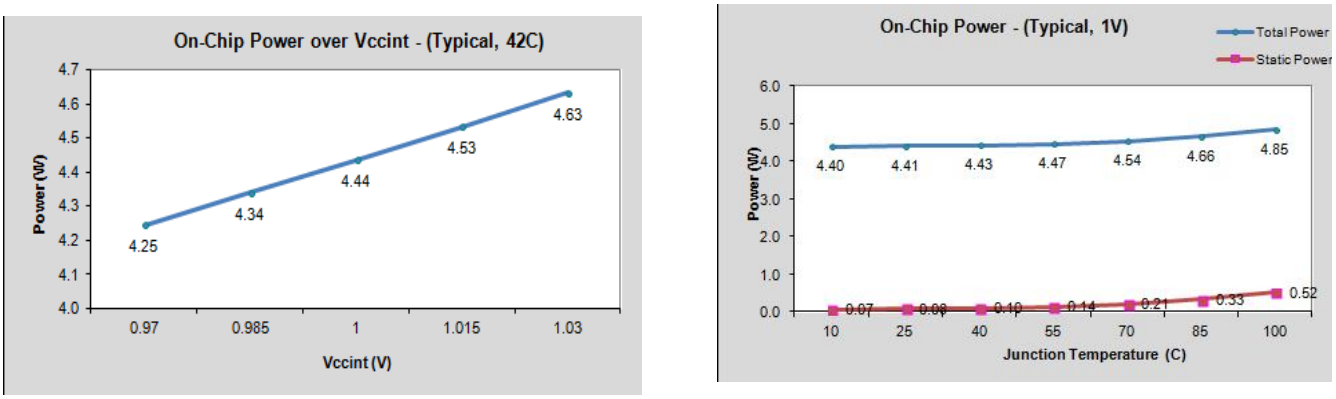


Fig. 16 Power Consumption for reversible 16-bit adder-subtractor using WG gate

C. Design 3

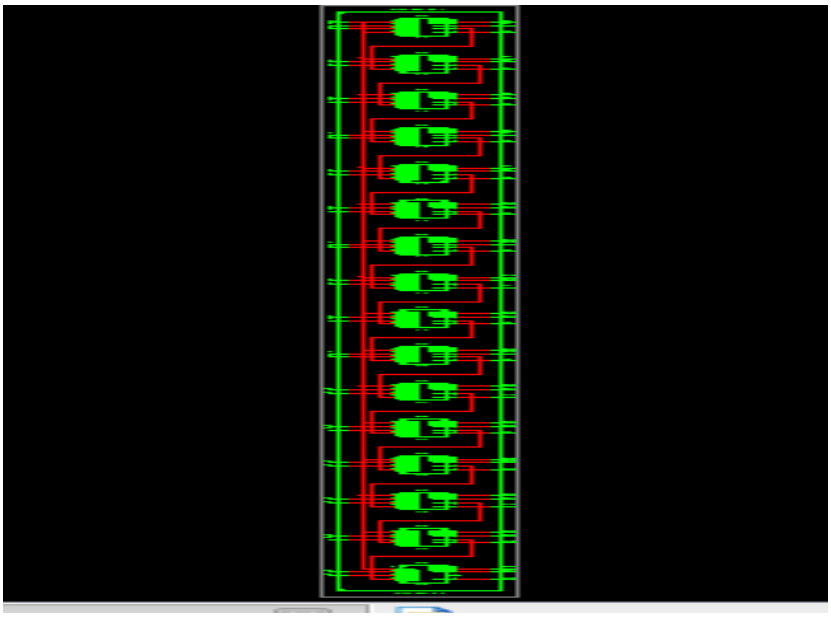
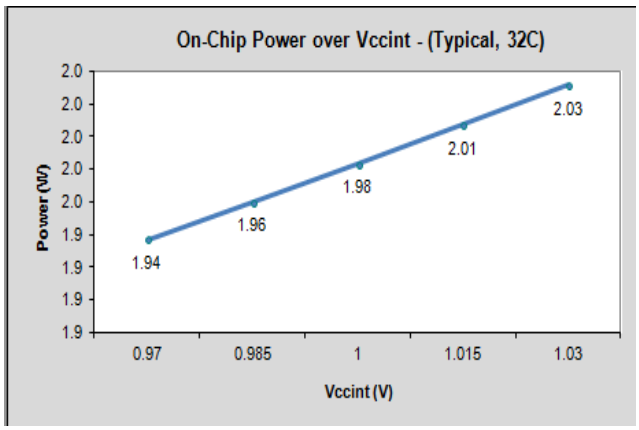


Fig. 17 Proposed design of 16-bit adder-subtractor using DKG gate



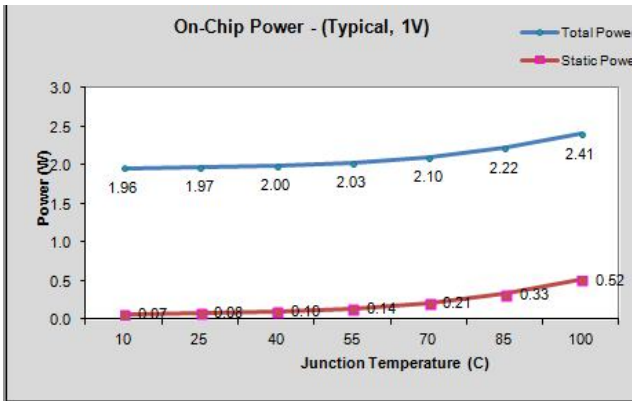
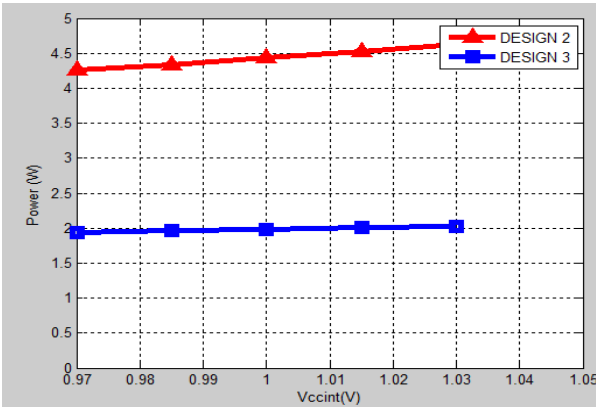


Fig. 18 Power Consumption for reversible 16-bit adder-subtractor using DKG gate



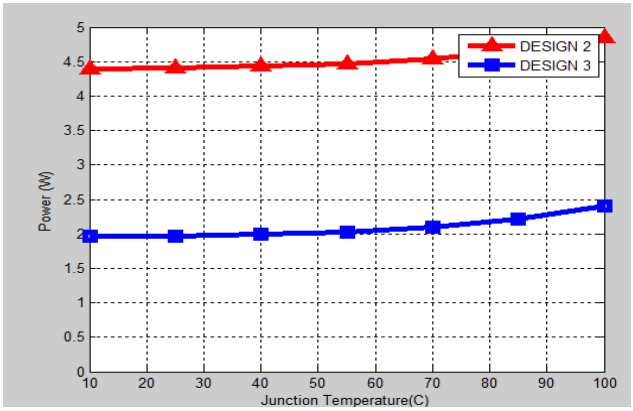


Fig. 19 Comparative results of power consumption graph for proposed design 2 and design 3

Table 1: Comparison of proposed work with existing work.

Sr. No.	Parameters	8 bit adder-subtractor design		16 bit adder-subtractor design	
		Proposed	Existing [16]	Proposed	Proposed
1.	Quantum cost	48	56	112	96
2.	Power consumption(W)	0.091	3.643	4.436	1.983

V. CONCLUSION

Reversible logic is an emerging technology which will lead to lesser power consumption and no power loss. In this paper 8-bit and 16-bit adder-subtractor circuits are designed using WG gate and DKG gate. Table 1 demonstrates that proposed design is better than existing design in terms of quantum cost and power consumption. The quantum cost of 8-bit adder-subtractor design using DKG gate is 48 and its power consumption is 0.091W whereas the quantum cost of existing design is 56 and its power consumption is 3.643W, the quantum cost of 16-bit adder-subtractor using WG gate is 112 and its power consumption is 4.436W, quantum cost of 16-bit adder-subtractor using DKG gate is 96 and its power consumption is 1.983W. Hence the proposed circuit is better than existing circuit in terms of quantum cost and power consumption.

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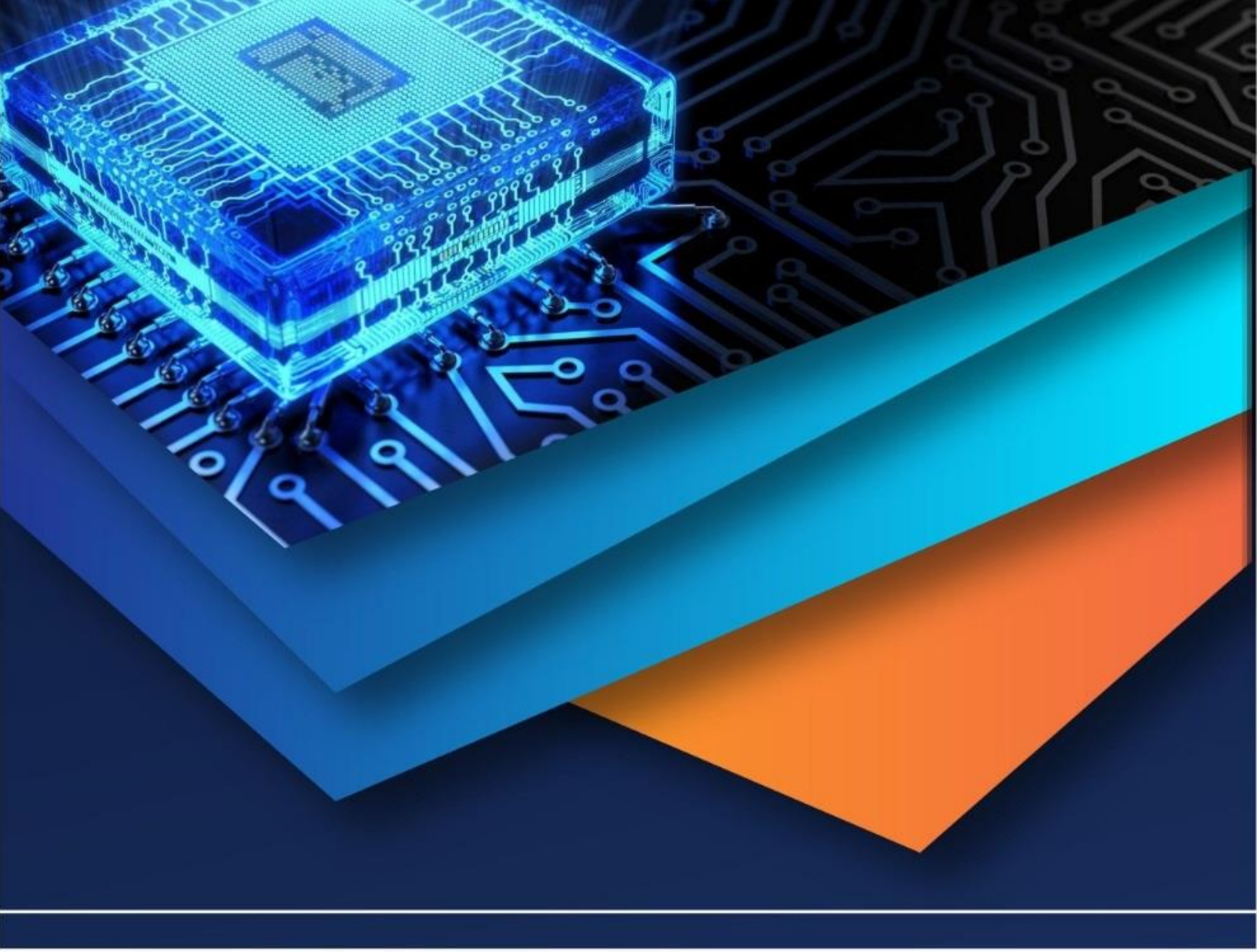

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