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A 2.6-mW 4-b 4.8-GS/s Dual-Edges-Triggered Time-Based Flash ADC

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Abstract-This paper proposes a 4-b 5-GS/s time-based flash ADC in 45-nm digital CMOS technology, which utilizes both rising and falling edges of the clock for sampling and quantiza-tion. A dual-edge-triggered scheme reduces the dynamic power consumption of a voltage-to-time converter and the clock buffers by half. We doubled both the reset and the available regeneration times by interleaving the time comparators. The ADC has a low input capacitance and the calibration circuit is included on-chip for suppressing various mismatches. The prototype running at 5 GS/s consumes 2.6 mW from a 0.8-V supply and achieves a signal-to-noise and distortion ratio of 26.19 dB at Nyquist.

Index Terms— Analog-to-digital converter (ADC), flash, time-based dual-edge-triggered.

I. INTRODUCTION

The required bandwidth of communication systems has grown rapidly, and applications such as the serial links need GS/s ADCs with great power efficiency and small area. Flash ADC is known as the fastest single channel ADC architecture which relies on the parallel operation of comparators. However for higher resolution, the number of comparators increase exponentially, which not only leads to a large area occupation but also significant amount of power consumption [1]. Another type of ADC architecture relying on massively parallel operation is the time-based ADC which mainly consists of time-to-digital converters (TDCs). The simplest form of a TDC is a digital counter. Thus, both the speed and the energy efficiency are greatly limited by
the number of bit counters that also expand rapidly with the bit resolution. While time-domain converters have been widely adopted in sigma delta ADCs for their 1st order noise shaping characteristic [2], [3], in multi-bit SAR ADC for replacing multiple comparators [4] or in the digital slope SAR-assisted ADC, the required long counting period [5] limits their operation in GHz applications.
Thanks to technology scaling, both flash and time-based architectures experienced significant advancements on both speed and energy efficiency

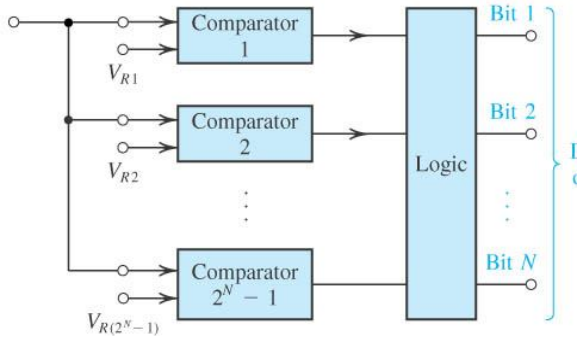

Fig .1 Flash analog to digital converter

Due to the small device size and less logic gate delay. The paper in [6] reports a 4.8 GS/s flash ADC with offset calibration in 32nm SOI CMOS technology achieving a Walden figure of merit (FoM) [7] of 59 fJ/conversion-step. Furthermore, with massively parallel time-domain sub-converters in [8] the sampling speed of the time-based ADC can reach up to 4 GHz; however, the signal bandwidth is only 20 MHz and the SNDR greatly limited by the mismatch between the sub ADCs.
It can be observed from the state-of-the-art ADC survey in Fig. 1, the limitation of the FoM of the single channel full flash ADC designs is mostly within 10 pJ-100 fJ/conversion-step. The Nyquist sampling rate (f_{snyq}) can reach 8 GS/s at high values of the FoM. On the other hand, time-based ADC designs have greater limitation on speed and are only able to achieve 75 MS/s with a 200

fJ/conversion-step FoM. In this work, we would like to explore the possibility of time-based ADC operation beyond GS/s (~5GS/s) achieving a competitive FoM when compared with other designs in the voltage domain.

In this paper, we propose a time-based flash ADC which utilizes both raising and falling edges of the clock to sample and quantize the input signal, thus reducing by half the required clocking frequency to save power. The mismatches induced by routings and different clock edges are handled by careful layout and calibration technique. Besides, rather than utilizing the digital counter, the quantization process obtained by time-based comparators in a flash manner can greatly enhance the speed. Further, we embed the time references in each time comparator with accuracy ensured by an on-chip calibration circuit. The prototype realizes in 45nm CMOS technology and achieves 4.8 GS/s at 0.8 V supply with a core area of only 0.004 mm^2. The Nyquist SNDR is 26.19 dB and it consumes 2.6 mW power, yielding a Walden FoM at Nyquist of 94.6 fJ/conversion-step. The proposed ADC achieves the highest sampling

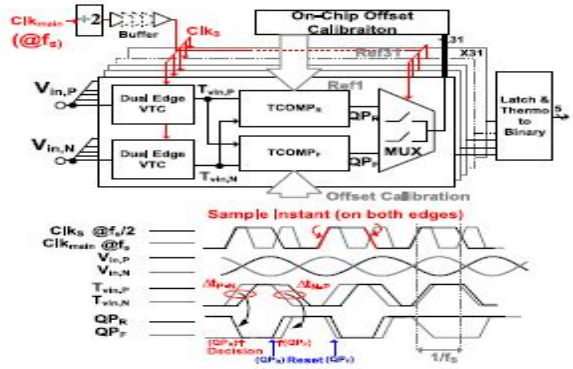

Fig.2. . Proposed ADC architecture

rate among the time-based ADCs. When comparing with the other flash ADCs in a similar resolution (5-6b), the prototype achieve a competitive FoM in 3-5 GHz sampling rate. The paper is organized as follows. We first introduce the proposed time-based ADC architecture in section II. Section III describes the circuit implementations of the main building blocks. Next, we present a design analysis in detail in Section IV. Finally, we discuss the measurement results in Section V.

II. PROPOSED TIME-BASED ADC ARCHITECTURE

Fig. 2 illustrates the functional block and timing diagrams of the ADC. The 5b prototype consists of a frequency divider, 31 dual-edge-triggered voltage-to-time converters (VTCs), 31 ris-ing and falling edge time comparators (T_{COMPR} and T_{COMPF}) followed by 2-to-1 multiplexers (MUX) at their outputs, a latch, a thermometer-to-binary decoder and an on-chip calibration circuit. Instead of being processed in the voltage domain, the differential inputs ($V_{in,P}$ and $V_{in,N}$) are first sam-pled and converted simultaneously to time ($T_{vin,P}$ and $T_{vin,N}$), by 31 VTCs during both the rising and falling edges of the sampling sub-clocks (Clk_S). Clk $_S$ is at half the fre-quency of the main clock (Clk_{main} = 5 GHz) from the frequency divider. The racing condition between $T_{vin,P}$ and $T_{vin,N}$ as a time difference on both the rising and falling edges (t_{P-N}/ t_{N-P}) can be detected and regenerated into a logic decision (QP_R/QP_F) by T_{COMPR} and T_{COMPF}, respec-tively. All the 62 time comparators in each slice embed their corresponding time references. The MUX multiplexes both time comparators' outputs which follows by a thermometer-to-binary decoder to decode to 5b from the total 31 units' outputs. Furthermore, we adopt on-chip foreground

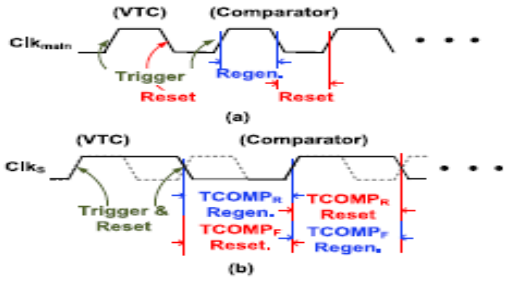

Fig. 3 (a) timing diagram for a conventional TDC and (b) proposed

Fig. 3 (a) shows the timing diagram for a conventional TDC or voltage comparator, where they utilize only single edge of the clock (rising in this example) to trigger and obtain the decision while the other edge serves to activate the reset procedure. This not only

reduces the regeneration time but also induces an extra switching activity with no quantization information. Both the available conversion time and power are wasted in the reset phase. In the proposed design (Fig. 3 (b)), we adopt both edges to trigger and reset the VTCs, and their corresponding comparators to give decisions. This provides an relaxed regeneration time for the comparators and reduces the switching frequency of the VTCs and their following buffers by half, thus saving dynamic power. Also, two interleaved comparators, triggered between the rising and falling edge of the Clk_S, have their regenerative and reset times doubled.

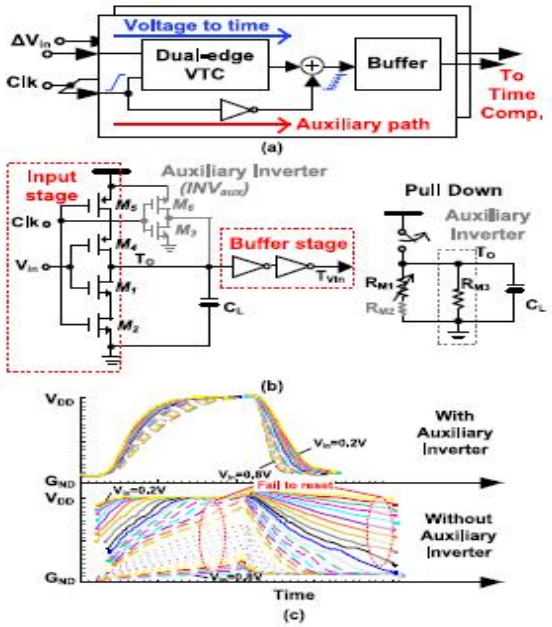

Fig.4. Conceptual block diagram and schematic and © output signal behavior

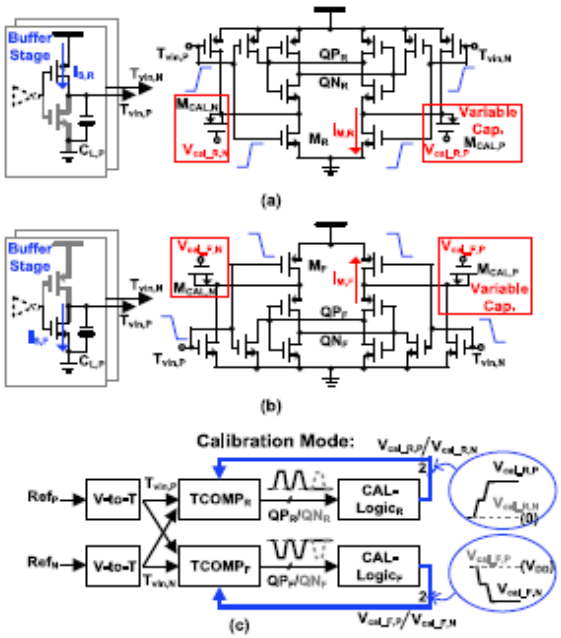

Fig..5. Circuit schematic of time comparator

A simulation is setup to show the power saving of the proposed architecture comparing with conventional approach. Two cases are depicted in Fig. 4 (a) and (b) respectively. Both cases adopts the
same $TCOMP_R$ but the VTCs in conventional approach (Fig. 4 (b)) are reconfigured to single-edge while all the size of transistors are kept the same. Furthermore, the clock generator in the presented design con-sists of a frequency divider while the conventional

approach only needs an inverter chain. From the pre-layout simulation with f_S = 4.8 GHz, the power saving of the dual-edge scheme is around 2.16 times from the conventional one in total, where the clock generator save around 3.8 times and VTC+TCOMP save around 1.5 times. The clock generator save more than 50% power as its power also relate to switching frequency. While only VTC's power is saved and the TCOMP's power is the same in both case, the saving is less than 50%. But when considering the clock generation and buffer circuits, the total power saving is more than 50%.

III. CIRCUIT IMPLEMENTATION AND LAYOUT CONSIDERATIONS

A. Dual-Edge-Triggered Voltage-to-Time Converter

Fig. 5 (a) depicts the conceptual block diagram of a key block of the architecture that is the dual-edge-triggered VTC. This circuit contains both sampling and voltage-to-time (V-to-T) conversion functions, and should simultaneously provide a high speed operation with enough driving capability to the following stage. During both the rising and the falling

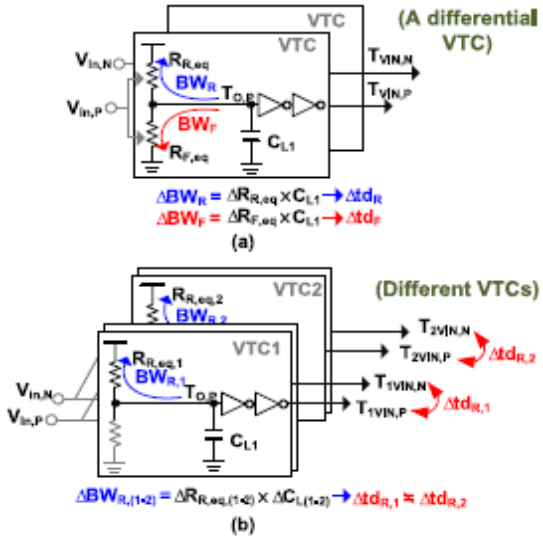

Fig..6 Bandwidth match effect on the proposed design

edges of the clock signal (Clk), a pull-up and pull-down network converts the voltage input difference (V_{in}) to a time difference at the output of the dual-edge-triggered VTC. An assisted path from the inverted version of the clock signal feedforwarded to the VTC's output helps to speed up the V-to-T process. Then, the time difference is buffered to drive the following stage for time comparison.

Fig. 5 (b) illustrates a circuit schematic (single-ended) of the dual-edge-triggered VTC. The input stage includes two pull down transistors (M1 and M2) and pull up transis-tors (M4 and M5) with gates connected to the input (V_{in}) and the clock (Clk), respectively. M2 size is 4× larger than M1 for high speed, and INV_{aux} is induced in parallel to the input stage with clock (Clk) control to further increase the VTC's speed and eliminate the inter-symbol interference (ISI). Unlike the clocked-comparator, Clk signal is connected to both M2 & M5 to pull up and then down the output (T_O) alternatively; while, V_{in} modulates the pulling resistance thus changing the rise/fall time.

Fig. 5 (c) illustrates the difference between the VTC's outputs with and without the auxiliary inverter (INV_{aux}). Without INV_{aux}, the voltage-to-time conversion can occupy a long period dependent on the input voltage. Furthermore, the output of the VTC fails to reset when the input voltage is 0.4 V. With INV_{aux}, the conversion speed is enhanced with a penalty of smaller LSB time difference. While time comparators are often adopted in high resolution ADCs [10] with more than 10b resolution due to their low noise nature, the finer LSB step is not problematic in this 5b design.

When the input stage is in a pull down condition without auxiliary inverter, the discharging time constant τ mainly depends on the equivalent on-resistance of M1 (when M2>>M1) and the capacitive load (C_L), which can be expressed as (ignoring the channel length modulation) [11],

$$\tau = {}^{R}\text{eq,M1} \cdot {}^{C}L$$

$$\frac{3}{} \frac{{}^{C}L\ 1\ {}^{V}D\ D}{} \approx 4\ (W/L)_1(\mu C_{ox})_n \quad V_{in} - V_{thn} - V_{DSATn}/2 \quad V_{DSATn} \qquad (1)$$

where $V_{D,SATn}$ is the drain source voltage when the velocity saturation occurs, W_1 and L_1 are the width and length of M_1, μ_n and C_{oxn} are the mobility and the oxide capacitance of the NMOS transistor, respectively. V_{in} and V_{thn} are the input voltage and the threshold voltage of M1, respectively. V_{DD} is the supply voltage. When a small input swing is used, the overdrive voltage (V_{in}-V_{thn}) of M1 is small which makes it not able to fully turn-on and leads to slow discharging speed. (the longest in this design) is about 77 μm long and 0.6 μm wide in the top thick metal layer which has a nominal resis-tance R_{nor} and capacitance of ∼60 and ∼50 fF, respectively. While the standard deviation of the parasitic capacitance due to the interconnection can be as small as 0.1%, the resistance often can be up to around 0.2% (structure B in [13]). Even the wiring structure in [13] is different from this design, it can be found that the mismatches are mainly depended on the number of VIAs and area in [13]. We pick the worst reported structure in [13] as our reference which has >13× R_{nor} than our design for worst case consideration. When, we consider the variation on the routing resistance which can be found as,

$$\sigma_{R,con} = R_{nor} \cdot 0.2\% = 60 \cdot 0.2\% = 0.012 \qquad (6)$$

where R_{nor} is the nominal routing resistance, W d L is the routing width and length, respectively. The variation induced by routing is only 0.088 which is very small when comparing it with device mismatch. Thus, this contribution on the overall mismatch is negligible.

IV. CIRCUIT NON-IDEALITIES

Various circuit non-idealities, such as clock skew, bandwidth mismatch and VTC's nonlinearity affect the performance of high-speed data converters. The clock skew and bandwidth mismatch error is mainly induced by clock distributions, mismatch between the basic cells and in our specific case by the different rising and falling voltage-to-time sampling paths. We minimize the clock routing mismatches through a symmetrical floorplan, a careful layout of basic cells and their common centroid placement alleviate mismatches. However, the timing error due to the utilization of different clock edges can be problematic. Therefore, the clock circuit design and relative considerations are one of the most challenging considerations of the converter. Despite the limited resolu-tion at very high speed the above errors can be substantial and in order to limit their effect it is necessary to adopt calibration.

A. Clock Skew and Aperture Error

Even though the floorplan can ensure a certain level of matching between the clock and the input routing to the VTCs, the process and device mismatches can induce both timing and bandwidth mismatches similar to voltage domain interleaved sampling. Besides, the variation on sampling instant in differ-ent VTCs causes aperture error similar to flash ADC without sampling. First, we discuss the clock skew error.

The sampling clock is generated from a frequency divider whose output passes through a chain of buffers to reach different VTCs. The process and mismatch variation yields an unsymmetrical rising and falling time deviation, thus leading to image spurs in the spectrum. Since the proposed design targets are 5 GS/s with 5b, the clock skew error between the rising and falling edge as well as among the VTCs must have a standard deviation less than [14],

where M is the number of channels, N is the bit resolution and f_{in} is the Nyquist input frequency. This imposes a boundary of ∼1% error on the 50% duty cycle. Under process and mismatch variation, both the frequency divider and the buffer chain suffer and we will analyze them separately next.

Fig. 10 (a) shows an example in the SF (N-slow-P-fast) corner with 4 inverters in series. Both rising and falling edges of the clock (Clk) pass through 2 slow corner NMOS (S) and 2 fast corner PMOS transistors; therefore, they experience similar variations under the corner condition. On the other hand, the rising and falling edge of Clk passes through various transistors with different device mismatch, all devices in the clock path induce mismatch as illustrated in Fig. 10 (b). Such mismatch error can only be suppressed by enlarging the size of the devices or reducing the number of buffers from the source clock to the VTC. However, the former solution can lead to large power consumption and the latter is not practical due to large routing parasitics. Based on a double-edge-trigger technique, the power consumption from the buffers is inherently reduced by two, and enlarging the devices' size becomes acceptable. It is worth noting that the most problematic scenario is when the NMOS and PMOS transistors are in the SS corner. The slope of both edges are the gentlest thus having the highest sensitivity to the mismatch. The scenario discussed above is not only applicable to the edges mismatch between rising and falling edges but also among the VTCs. In the proposed design, the clock

source passes through 4 inverters to the VTC and each has a fan-out of 2. The standard deviation of the sampling time difference between rising and falling edges and among the VTCs under the SS corner should be within the target obtained in (5),

B. Bandwidth Mismatch

Since the VTC's sampling is based on signal-modulated resistance at the charge/discharge path as indicated in (1), the bandwidth mismatch between both paths is directly reflected as different time constants among the rising and falling edges of the VTC (case 1), and among the VTCs in different slices (case 2). Fig. 11 (a) depicts the bandwidth mis-match between the rising and falling edges within a differential VTC pair (case 1). The rising and falling path bandwidth mis-matches (BW_R/BW_F) are mainly due to the device mismatch causing variation on the equivalent on-resistance of the input transistors ($R_{R,eq}/R_{F,eq}$). Such mismatches can be considered simply as a delay (td_R/td_F) since they are originated from the RC time constant. Such delay variations are equivalent to time offset and possible to be corrected by the calibration circuit.

C. VTC Nonlinearity

Nonlinearity of the VTC limits the performance of the conversion accuracy. Therefore, the VTC is often placed in the backend of a sub-ranging type of ADC which handles a smaller input range [4].

Due to the calibration circuit and the auxiliary inverter, this design has better tolerance to the nonlinearity of the VTC. As the auxiliary inverter greatly reduces the ISI, the nonlinearity of the VTC can be addressed by the calibration circuit. Fig. 12 shows the conceptual voltage-to-time characteristic of the rising and falling paths of the VTC and their corresponding adjustment circuit. Since the rising and falling edges utilize different transistors for

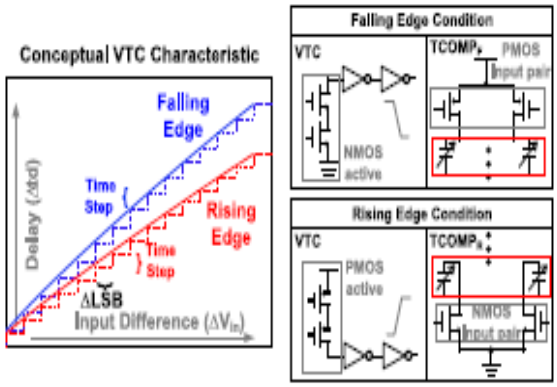

Fig.7.. Nonlinearity of the VTC

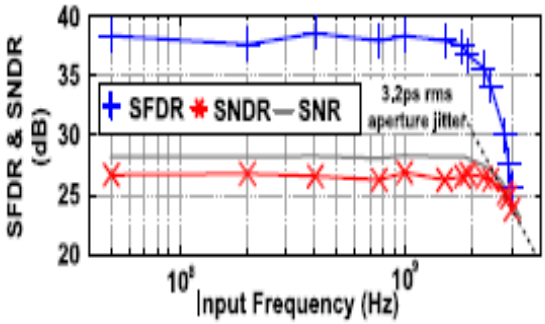

Fig.8 . SNDR and SFDR across different input frequencies

conversion, their V-to-T curves are different. With large input voltage difference (V_{in}), the time difference (t_d) is monotonically increased but the time step is highly nonlinear. The nonlinear time step (in the same edge and also between the different edges) is corrected at the time comparator ($TCOMP_R$ and $TCOMP_F$) which can be explained as following. During calibration, calibration reference voltages is apply at the input of the VTC. Then, the reference voltages convert to delay by the nonlinear VTC. The time comparator adjusts its time reference according to the delay from the VTC's output. This procedure repeats 62 times for all the time

comparators. Therefore, the time references embedded in the time comparators is adaptively adjusted to best fit the nonlinear trip-points caused by the VTC.

V. EXPERIMENTAL RESULTS

Fig. 13 shows the microphotograph and layout of the ADC fabricated in ST 45 nm CMOS. It has a core area of 0.004 mm^2 and a total area of 0.096 mm^2 including calibration. The ADC full-scale input is 0.6 V_{pp} with a common-mode volt-age of 0.7 V. With 1 V supply, the power consumption is 7.8 mW operating at 5 GS/s (27% in clock buffers, 58% in VTCs and time comparators, and 15 % in the output buffers, latches, decoder and calibration DAC). The calibration is in the foreground and on-chip at the operating frequency (5 GHz). Fig. 14 illustrates the measured SNDR and SFDR versus the input frequency. The SNDR stays above 26.19 dB up to the Nyquist input and drop to 24.23 dB at 3 GHz input frequency. The estimated aperture jitter is around 3.2 ps_{rms}. The SFDR also stays quite flat up to Nyquist input even without the S/H circuit. This is due to the sharp rising and falling edges of the clock for VTC as well as the symmetrical routings. The ADC full swing is also carefully chosen to avoid a large 3rd harmonic in the design. The maximum DNL/INL are suppressed from 4.3/3.5 LSB to 0.83/0.79 LSB, respectively, with calibration depicted in Fig. 15. Fig. 16 shows the frequency spectrum with and without calibration at near-Nyquist-tone. The sampling frequency (f_S) is 5 GS/s, the input frequency (f_{in}) is 2.41 GHz and the output is decimated by 625x. The highest tone that appears in the spectrum is the image spur which is due to the mismatch between VTCs' rising and falling edges as explained in section IV-A. Other tones are caused by the residue offsets in the comparators. The performance of the ADC is mainly limited by SNR which causes by thermal noise of the VTC and time comparator as well as aperture jitter. 27 dB at low frequency input. At high input frequency, the aperture jitter with 3.2ps_{rms}, which is from the noise of the clock generator and the mismatch amount the VTC from front-end, the limits the SNR. Such jitter is estimated from the trend of the degradation on the SNR of the ADC at high frequency input. With technology scaling, the rising and falling time are improved which can benefit this architecture in terms of speed and linearity. Table II summarizes the ADC's performance and compares it with the state-of-the-art. We implement the core with all transistors without passive device but having low input capacitance 66.6 fF with the calibration implemented on-chip, resulting in a Walden FoM of 94.6 fJ/conversion-step. This prototype demonstrates a competitive FoM and achieves the best energy efficiency among high speed (>GS/s) time-based ADCs. Comparing with other time-based ADCs [15], [18] in term of design philosophy, the proposed ADC utilizes clock edges to generate time difference and directly latch this different in flash fashion which enhances the speed of the time-based ADC. While [15] performs the quantization in two steps and [18] quantizes the time difference with counter, their achieved speed or resolution is limited. Besides, both edges of the clock signal are utilized for conversion in this prototype that can save power comparing with conventional voltage-domain flash ADC designs [17].

VI. CONCLUSIONS

This paper presented a time-based flash ADC which shows the potential of utilizing time domain conversion in very high speed ADC designs. With the proposed dual-edge-triggered scheme, the power consumption of the VTCs and the clock buffer circuits are greatly reduced; therefore, the prototype can achieve competitive energy efficiency when compared with other voltage domain ADC designs. Through the cooperation among the calibration circuit and the interleaved rising and falling edges comparators, the design is able to operate at 5 GS/s with a 26.19 dB SNDR at Nyquist input. The achieved SFDR is 34.22 dB which is little bit worse than the simulation result in Table I. While results in Table I only considers the variation in the active components of the clock, the routing of the input and the clock signal can induce small overhead thus leading to a bit worse measurement result. The proposed architecture is also suitable for technology scaling due to its pure dynamic power characteristic and the utilization of only CMOS devices.

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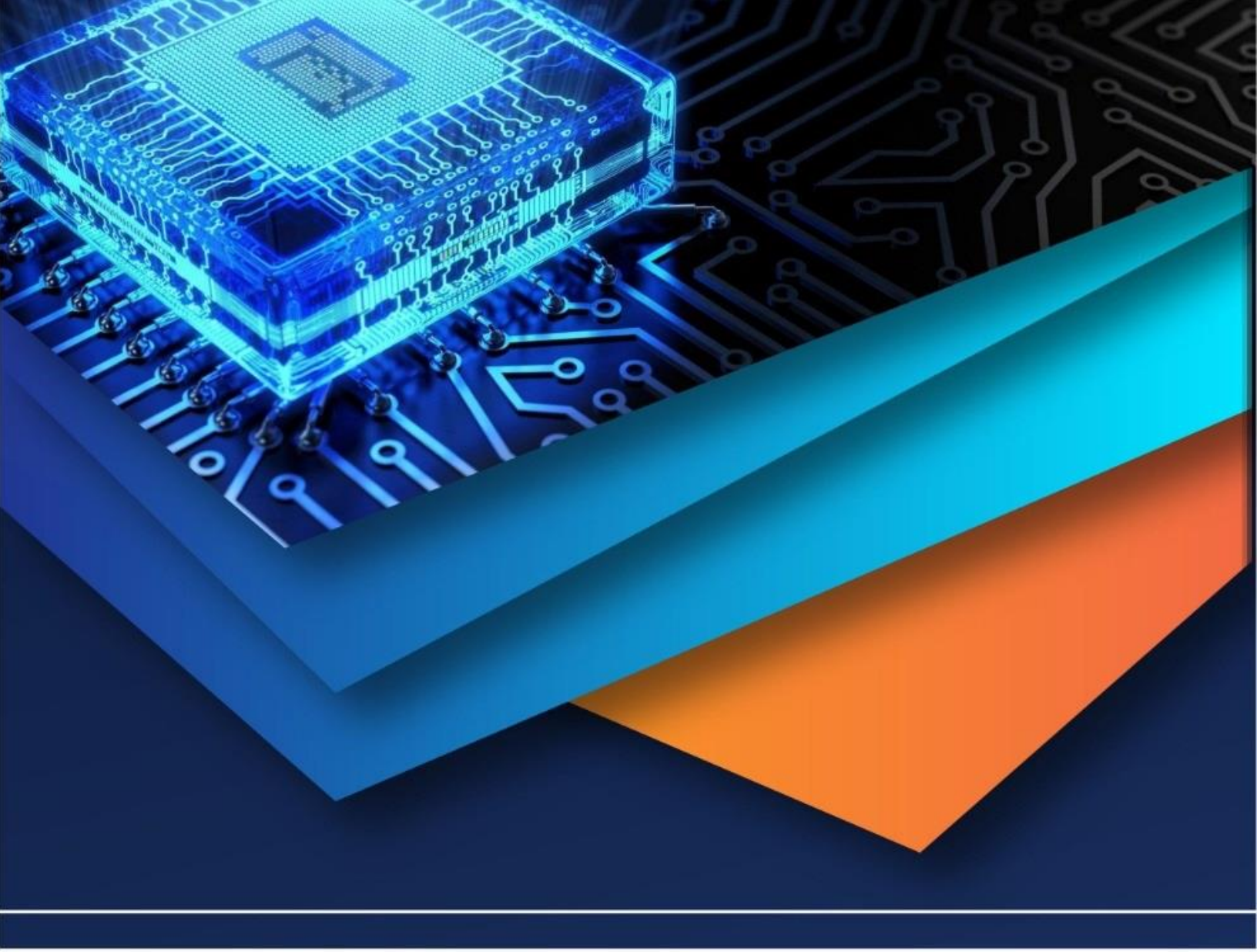

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