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Digital to Frequency Converting Flying Adder Architecture for Fractional Frequency Synthesis

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Abstract: Flying adder is an architecture which plays a vital role nowadays in our day to day life. It mainly helps to generate a fractional frequency from the given frequency. The main advantage in the architecture is it consist circuits which are pure digital. It can provide fast switching and reduce phase noise without effecting the phase locked loop bandwidth. Here Time average frequency concept is used , it makes clock generation easily. Combination of these two gives a Digital to frequency converter.

Keywords: Flying adder, time average frequency, phase locked loop (PLL), Digital to frequency convertor.

I. INTRODUCTION

Flying adder is a digital circuit for example multiplexer, flip flops and accumulators. Nowadays digital circuits are widely used than analog because these analog circuits are sensitive to environment. Finally we will get corrupted signal. Better to use less number of analog components to get spectrally pure results. Previously we came across different PLL's example integer PLL, fractional PLL, sigma delta PLL. To generate direct frequency integer PLL is used. To fractional multiple of given frequency fractional PLL is used. These are facing a problem of spectrum purity degradation. Flying adder eliminates all these drawbacks without effecting loop bandwidth.

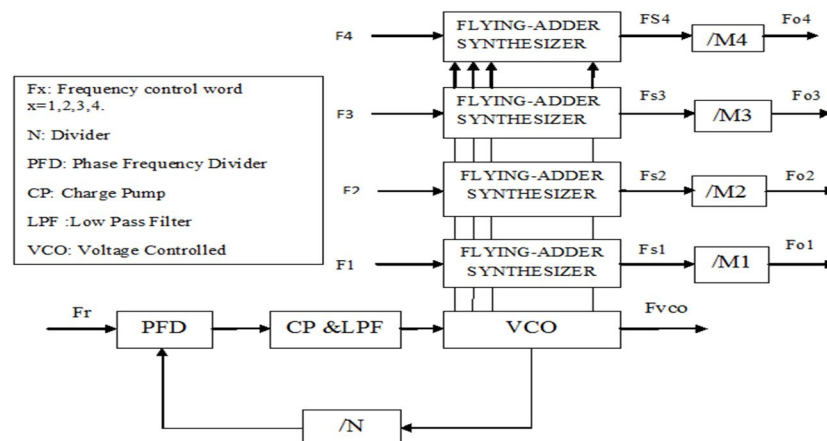


Fig . 1 ON-CHIP frequency generator using Flying adder's

II. FLYING ADDER AS ON-CHIP FREQUENCY GENERATOR

Direct period synthesis is also referred as Flying adder. Here Time average Frequency is used combination of these two concepts is known as digital to frequency convertor. By using this flying adder number of required PLL count in large circuits will reduce. For example consider only one PLL and take Flying adder's as many frequencies required as shown in fig .1 above.

III. FLYING ADDER ARCHITECTURE

Reference frequency is given to PLL from crystal oscillator. VCO present in PLL converts voltage to frequencies which are having same period with Δ phase difference. These VCO outputs are give as multiplexer input's as shown in fig.2 below .

B. Digital To Frequency Convertor

By these flying adder and time average frequency techniques a new component digital to frequency converter (DFC) comes into role. And it is shown in below fig. 7.

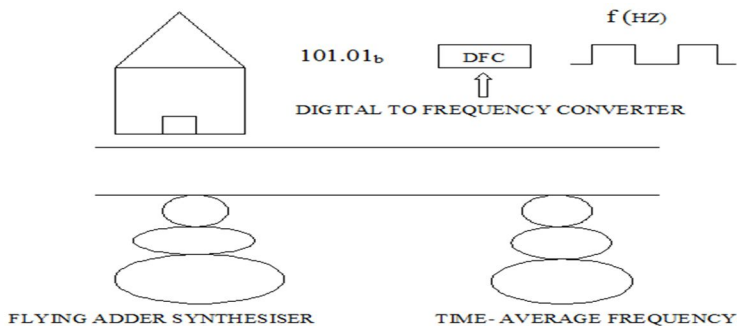


Fig 7. Digital to frequency converter

C. Output waveform:

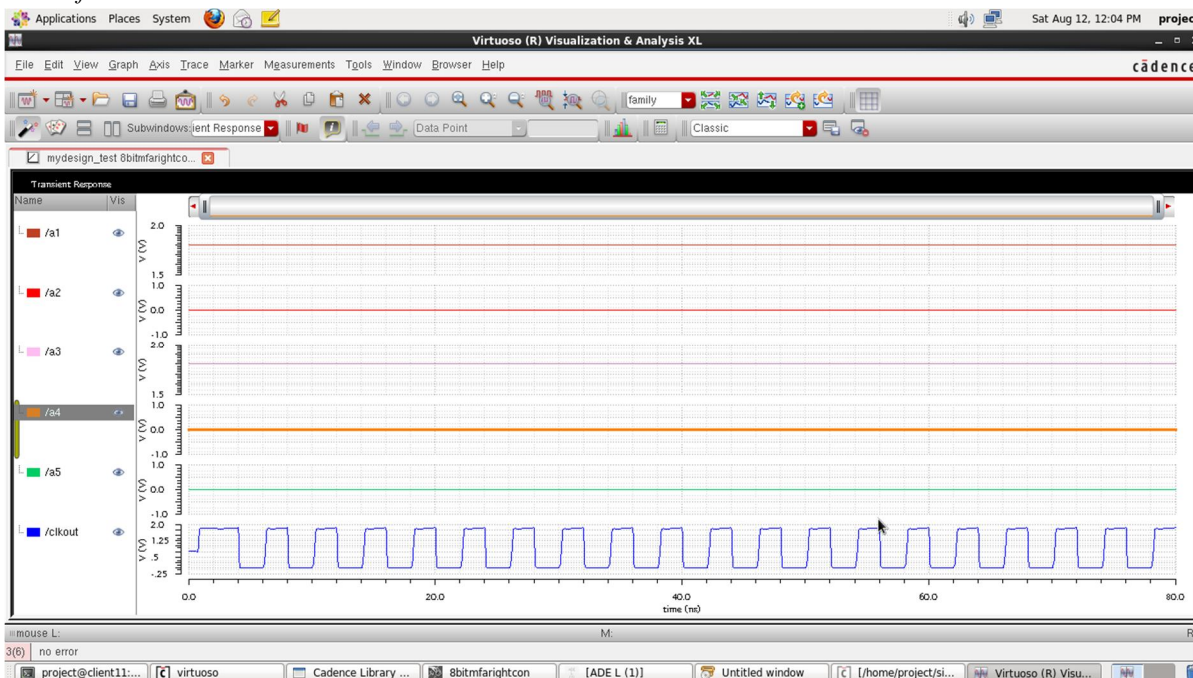


Fig 9. Digital inputs and it's frequency output

D. Results

Control word $A=101.00 \Rightarrow 5$, carry-in $CIN=0$, delay between two VCO signals $\Delta=0.401ns$

1) Theoretical Value

Time delay between two adjacent outputs

$$\text{output clock} = \text{control word} \times \Delta \times 2$$

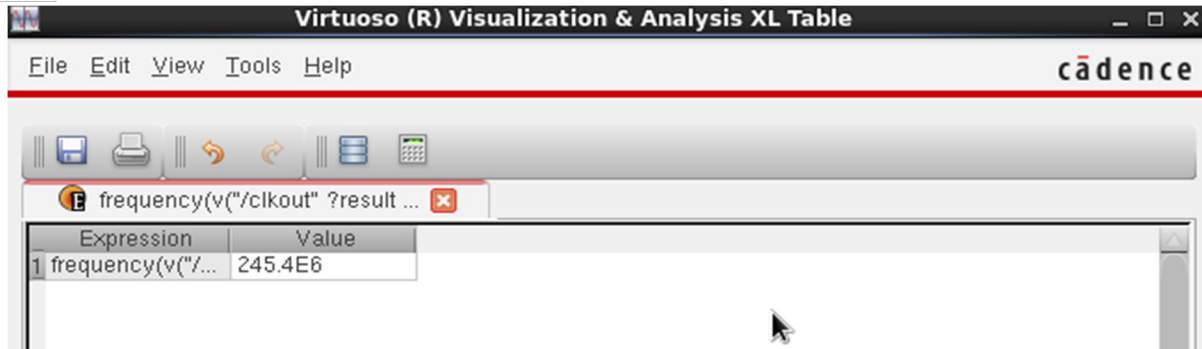
$$= 5 \times 0.401n \times 2$$

$$= 4.01ns$$

Desired output clock freq = $1/4.01ns = 249.37Mhz$

2) Practical Value

Output clock freq = $245.4Mhz$



Expression	Value
1 frequency(v(\"/clkout\" ?result ...)	245.4E6

VI. CONCLUSION

By these flying adder and time average frequency techniques a new component digital to frequency converter (DFC) comes into role. This technique is useful to get generate fractional frequencies very easily without facing difficulties like environmental changes as it is completely consist of digital circuits. This proposed technique improves frequency switching and phase noise. For generating large systems ON-CHIP frequencies this flying adder helps a lot to reduce area.

REFERENCES

- [1] H. Mair and L. Xiu, "An architecture of high-performance frequency and phase synthesis," IEEE J. Solid-State Circuits, vol. 35, no. 6, pp. 835–846, June 2000.
- [2] L. Xiu and Z. You, "A Flying-Adder architecture of frequency and phase synthesis with scalability," IEEE Trans. on VLSI, pp. 637–649, Oct., 2002.
- [3] L. Xiu and Z. You, "A new frequency synthesis method based on Flying-Adder architecture," IEEE Trans. on Circuit & System II, pp. 130–134, Mar. 2003.
- [4] J.M. Ingino and V.R. Kaenel, "A 4-GHz clock system for a high-performance system-on-a-chip design," IEEE Journal of Solid-State Circuit, vol. 36, no. 11, pp. 1693–1698, Nov. 2001.
- [5] C. Cao, Y. Ding, and K.O. Kenneth, "A 50-GHz phase-locked loop in 0.13- um CMOS," IEEE Journal of Solid-State Circuit, vol. 42, no. 8, pp. 1649–1656, Aug. 2007.
- [6] B. Goldberg, "The evolution and maturity of fractional-N PLL synthesis," Microwave Journal, pp. 124–134, Sep. 1996.
- [7] T.A.D. Riley, M.A. Copeland, and T.A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," IEEE Journal of Solid-State Circuit, vol. 28, no. 5, pp. 553–559, May. 1993.



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