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Implementation and Performance Analysis of OFDM Based DVB-T System Using Matlab and HDL Coder

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Abstract: ***DVB-T is a most extensively use standard for terrestrial Television transmission in the world. The OFDM has advantages of high spectral efficiency and inherent robustness against channel fading so it is used in DVB-T system. We investigate the performance of the OFDM based DVB-T systems for 2k mode for 4-QAM in terms SNR, and BER under AWGN, Rayleigh and Rician channels using HDL coder with five input audio and video by simulation. In this research work, DVB-T is implemented first using MATLAB and then VHDL code is generated using HDL coder according to European telecommunications standards institute (ETSI), EN 300 744 standard. Reason for converting MATLAB to VHDL code is less power consumption, MATLAB simulation Validation and floating point to fixed point conversion accuracy. Synthesis and Simulation of OFDM based DVB-T in 2K mode have been carried out using Xilinx tool.***
Keywords: DVB-T, OFDM, VHDL, HDL Coder, SNR, BER

I. INTRODUCTION

Digital Video Broadcasting-Terrestrial (DVB-T) is one of the mainstream terrestrial transmission standard which employs terrestrial as transmission media for MPEG-2 (Moving Picture Expert Group) digital television signal[1][2]. The MPEG-2 is able to compress a Television (TV) programme from 270Mbit/s to only 5 or 6Mbit/sec while maintaining excellent quality characteristics. The DVB-T system uses orthogonal frequency division multiplexing (OFDM) to send out compressed digital audio signal, video signal and data through a MPEG transport stream. Transport stream refers to data stream containing video / audio /data programme/s to be carried from the generating/broadcasting equipment to the users/viewers [3] [4]. Fig.1 shows the block diagram of DVB-T physical layer. OFDM based DVB-T can be used for both stationery and mobile reception. Because of high data rate transmission capability and robustness to multipath delay features of OFDM, it is suitable for DVB-T application [5] [6]. OFDM is composed by several carries (2K=1705 carriers) equally spaced in frequency, each one is modulated separately using quadrature phase shift keying(QPSK) or quadrature amplitude modulation(QAM) and transmitted in the 8 MHz TV channel, so each carrier is 4462 Hz far from its neighbor[7].

In digital broadcasting, there are no vision and sound carriers, so the power for each carrier is the same. In digital TV transmitter (DVB-T) a single transmitter may be used to carry 4 (or more) video/audio/data programme channels. DVB-T standard allows mobile reception and Single Frequency Network operation. DVB-T system permit the efficient utilization of available radio frequency (RF) spectrum, resulting in superior sound/audio and image quality and the chance of adding high definition (HD) pictures services[8].

The rest of this paper is organized as follows. Section II describes the proposed model. Section III describes generating VHDL code is described in. Simulation results are discussed in section IV and conclusion is given in section V.

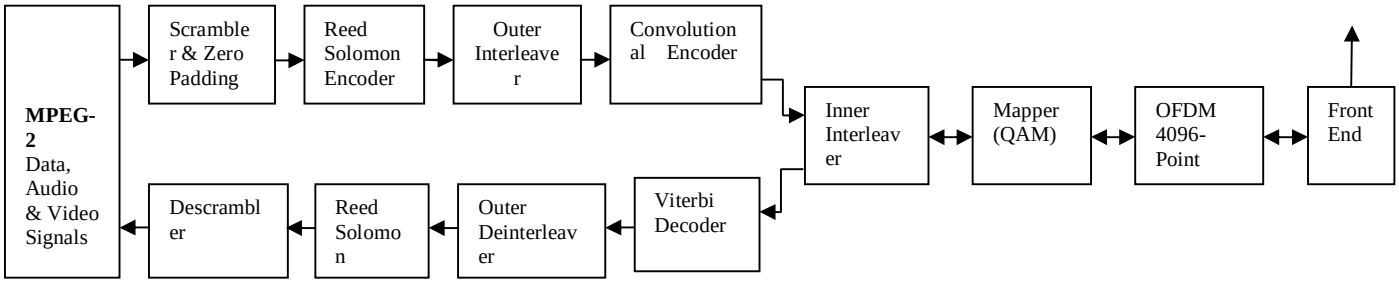

Fig.1 Block Diagram of the DVB-T System Physical Layer

II. PROPOSED MODEL

First the proposed model code is written and simulated in MATLAB and the BER performance of OFDM based DVB-T system for 2k mode in terms Signal to Noise Ratio (SNR) and bit error rate (BER) under AWGN, Rayleigh and Rician channels with inputs audio and video signals is analyzed. Fig.2 shows the block diagram of the OFDM system simulation model. Table 1 gives the parameters of Non- Hierarchical DVB-T under 2K mode for 8 MHz channel used for simulation [9]. The parameters varied in the simulations are given below.

A. Input: Five samples each for audio and video are used in the simulation to account the variations present due to compression techniques used and averages out the simulation limitation to a larger extent.

B. The Signal to Noise Ratio (SNR) of input is varied from 0 to 40 dB in steps of 5dB.

After this the MATLAB code is converted into very high speed integrated circuit hardware description language (VHDL) code using HDL coder from MATLAB toolbox. Reason for converting MATLAB to VHDL (output observation) is less power consumption, MATLAB simulation Validation and floating point to fixed point conversion accuracy. The generated VHDL code is synthesized and simulated using Xilinx tool. The BER performance is analyzed. Also power consumption, execution time and conversion accuracy is analyzed. The generated VHDL code sticks to a clean HDL coding style that allows architects and designers to quickly customize the code if needed. The test bench feature increases confidence in the accuracy of the generated VHDL code and saves the time spent for implementation of test bench. HDL Coder validates the build with the proposed fixed-point types and generates a fixed-point design. HDL Coder simulates the fixed-point design with the original test bench compares the output to the original floating-point design output.

The main models used to verify the hardware design are i. Register transfer level (RTL) model ii. Technology schematic diagram model. Register transfer level (RTL) model provides the synthesizable HDL model and presents the efficient architectural level description of the algorithm implemented in an VHDL language. Technology schematic diagram model gives the representation of components of a system through abstract and graphic symbols.

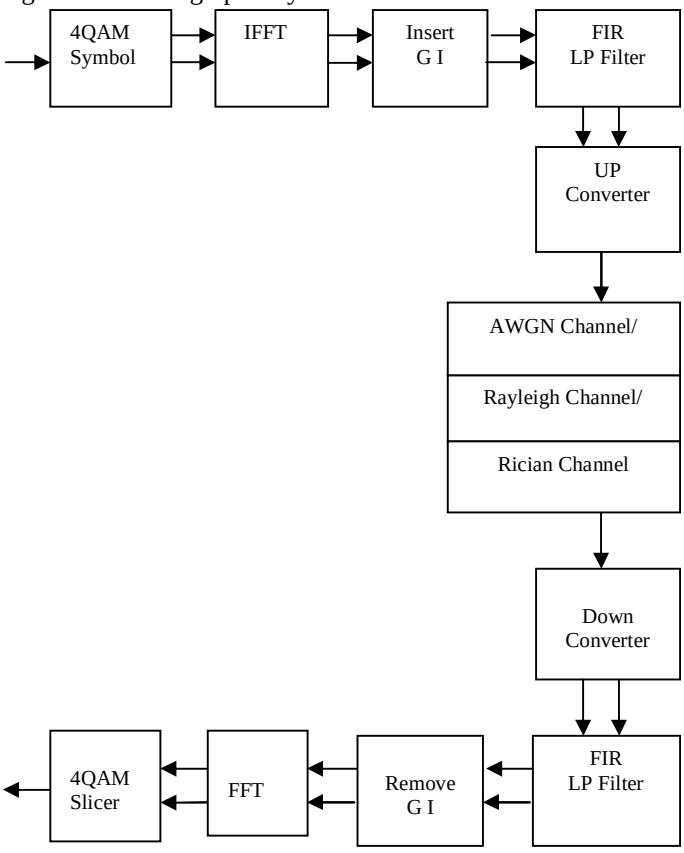

Fig. 2 Block Diagram of the OFDM Simulation Model.

III. GENERATING VHDL CODE USING HDL CODER

The Workflow Advisor in HDL Coder automatically converts MATLAB code from floating-point to fixed-point design and produces synthesizable VHDL code from MATLAB test script and function written for OFDM simulation model and also corresponding test bench is generated. The test bench with VHDL simulation tools is applied to drive the generated VHDL code and evaluate its performance. The generated VHDL code is optimized for hardware implementation. Fig.3 shows the flow Chart of HDL Coder Workflow. The steps involved in the generation of VHDL code from MATLAB is shown in Fig.4, Fig.5 Fig.6 and Fig.7. It is seen that using HDL coder .m file is successfully converted in .vhd file and by converting that .m file in .vhd file it is simple to analyze the hardware structure of generated module or it can be say that using HDL coder hardware analysis and Field-programmable gate array (FPGA) implementation can be successfully take place by generating a simple source code of MATLAB. So it can be concluded that the HDL coder generate an efficient way to convert floating point design of MATLAB code into fixed point design of VHDL code.

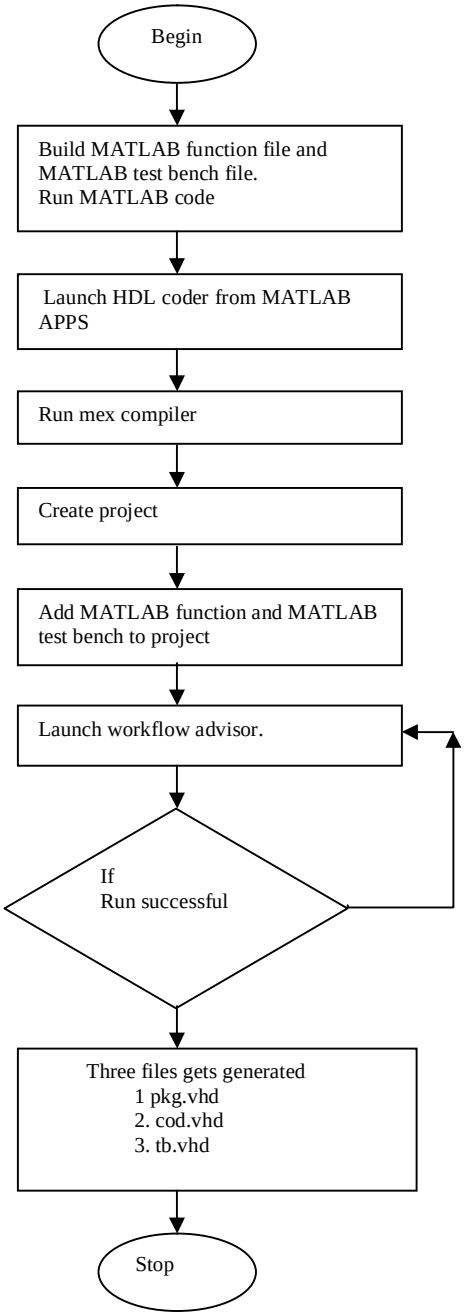

Fig.3 Flow Chart of HDL Coder Workflow.

Parameters	2K Mode
Elementary Period(T)	(7/64)µs
No. of carriers(K)	1705
Value of carrier number(K_{min})	0
Value of carrier number(K_{max})	1704
useful OFDM symbol period (T_u)	224 µs
Carrier spacing (1/ T_u)	4464Hz
Spacing between carriers K_{min} and K_{max} $[(K-1)/T_u]$	7.61MHz
FFT/FFT length	F_S = 4096
Simulation period	Rs = $4f_c$
Carrier frequency	f_c=q/T
Allowed guard interval (Δ/T_u)	1/4 1/8 1/16 1/32
Duration of guard interval (Δ)	512xT 256xT 56 µs 28µs 128xT 64xT 14 µs 7 µs
Total OFDM symbol period (duration) T_s= (Δ+T_u)	2560xT 2304xT 280 µs 252µs 2176xT 2112xT 238µs 231µs

Table 1 Parameters of Non- Hierarchical DVB-T [2]

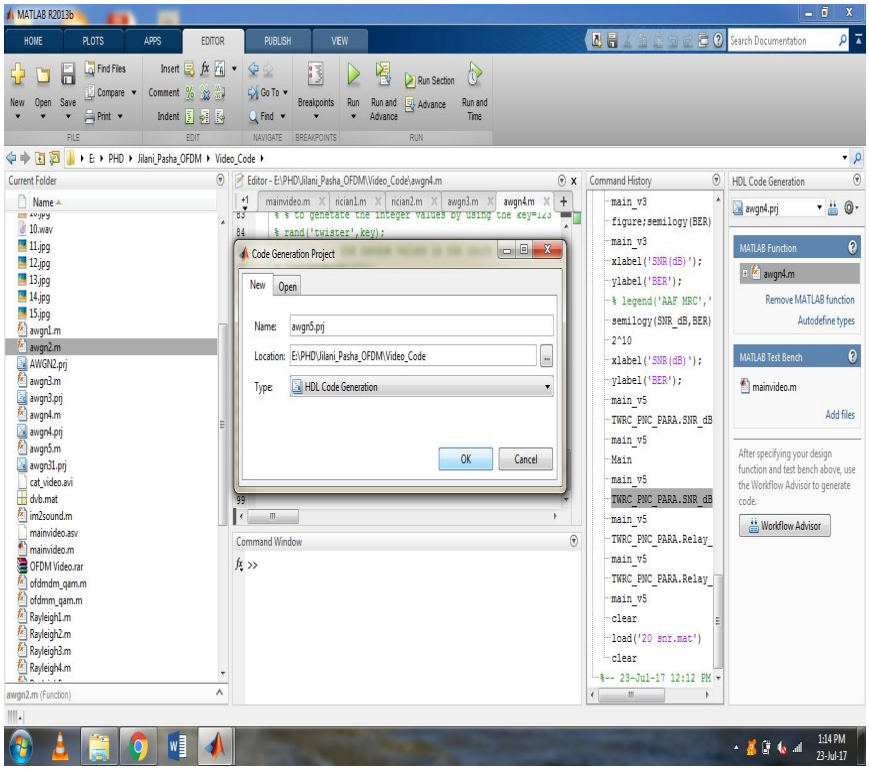

Fig.4 Code Generation Project Creation

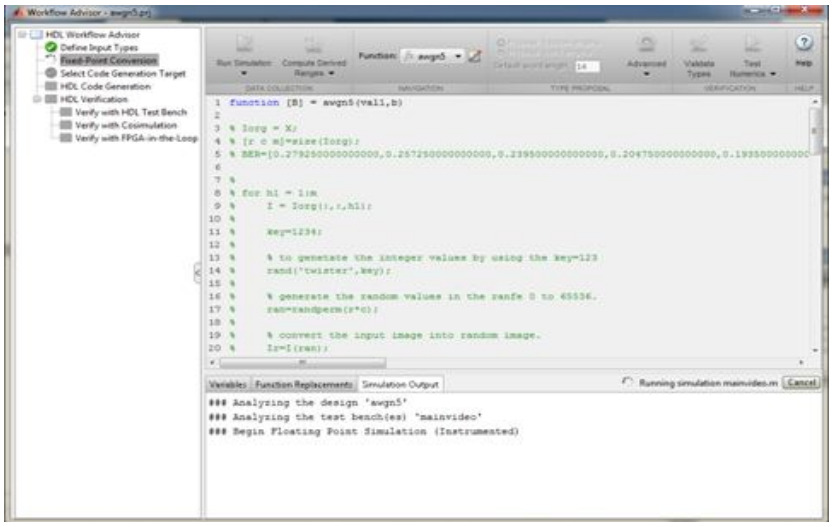

Fig.5 Fixed-Point Conversion Step of Workflow Advisor

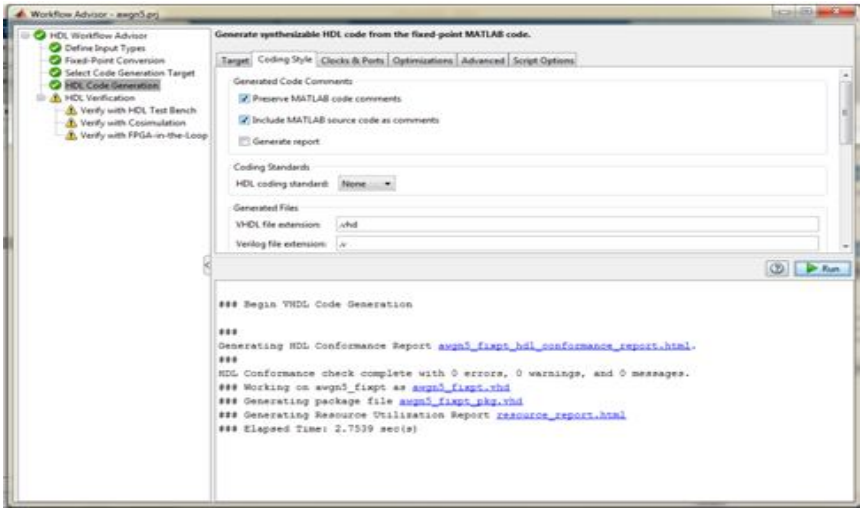

Fig.6 Generating Synthesizable HDL Code From Fixed Point MATLAB Code

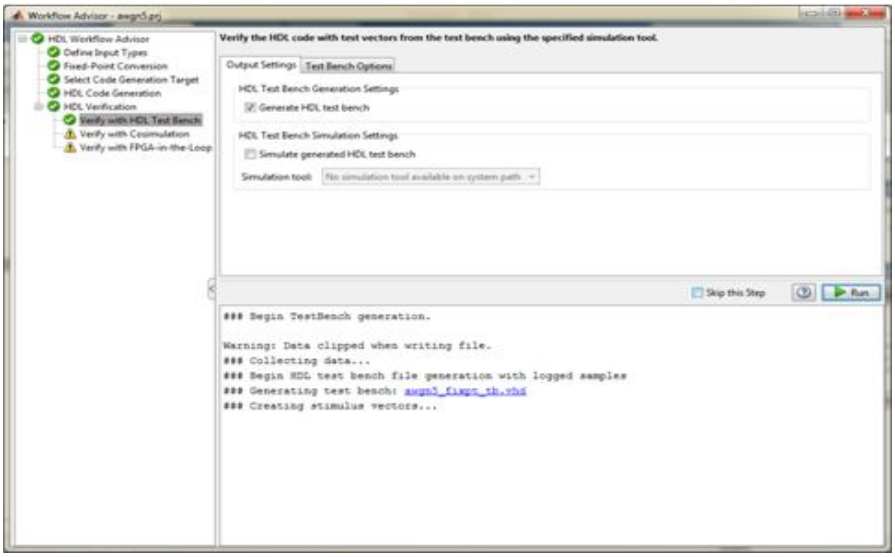

Fig.7 Verify the HDL Code with Test Vectors from Test Bench Using the Specified Simulation Tool

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IV. SIMULATION RESULTS & DISCUSSIONS

The proposed model simulation is carried out using Xilinx tool. The SNR is varied in between 0 to 40 dB. The implementation of VHDL code gives the RTL design and technology schematic view of code. Implementation results of proposed model in a VHDL indicate that the fixed-point design involves less hardware overhead, and achieves a maximum throughput. Finally, the performances of the fixed-point design are verified and simulation results demonstrate that the proposed fixed-point design provides an accuracy performance that is very close to that of floating-point (MATLAB) simulation counterpart.

A. Simulation of Audio signal.

The simulation is carried out using five different audio signals like as ‘aaj’,‘chaal’,‘chal’,‘chamak’ and ‘chouk’ to obtain the performance analysis of the DVB-T system

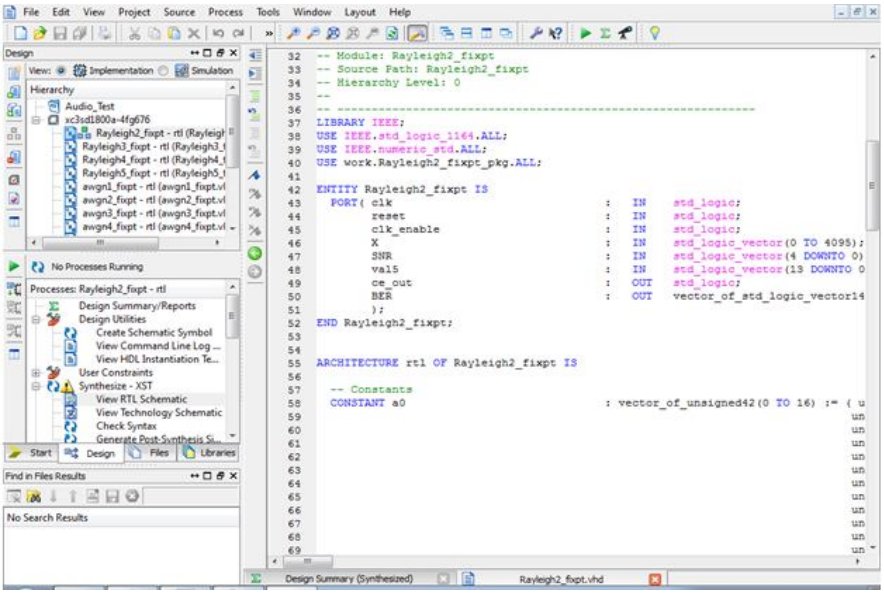

Fig.8 Generated VHDL Code for Audio Signal Input

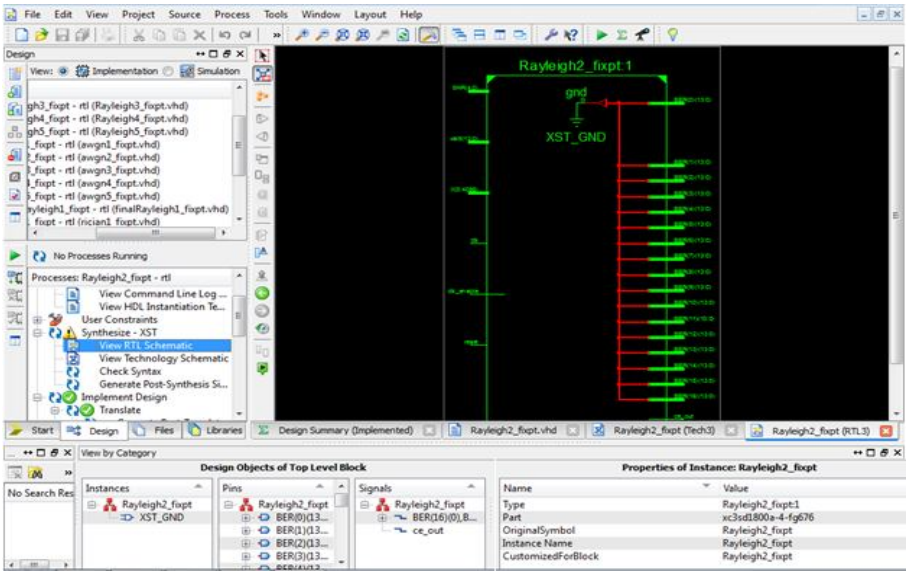

Fig.9 RTL Design

We see that by using HDL coder the floating point design of MATLAB code is efficiently converted into fixed point design of VHDL code. Also we see that HDL coder provides the elapsed time to execute the code and the generated VHDL code by HDL Coder from MATLAB function is portable, synthesizable as shown in Fig.8 and Fig.13.

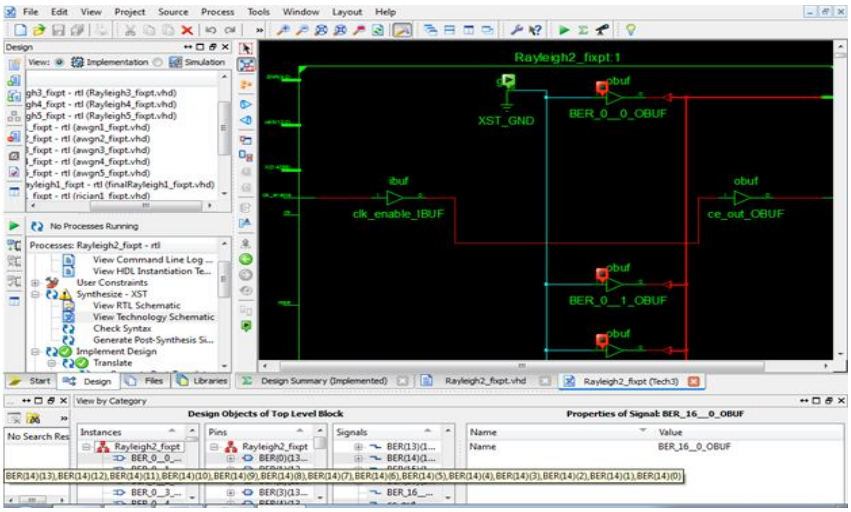

Fig.10 Technology View

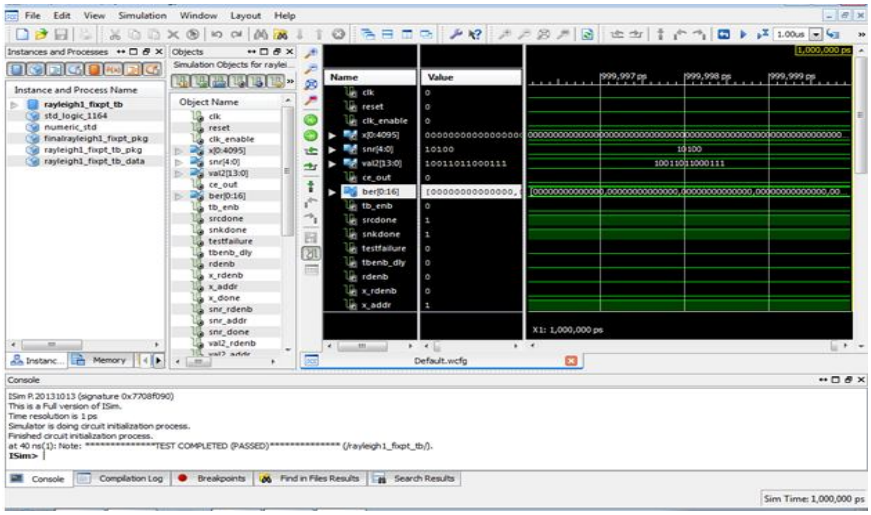

Fig.11 Simulation Result of SNR and BER Values in Binary

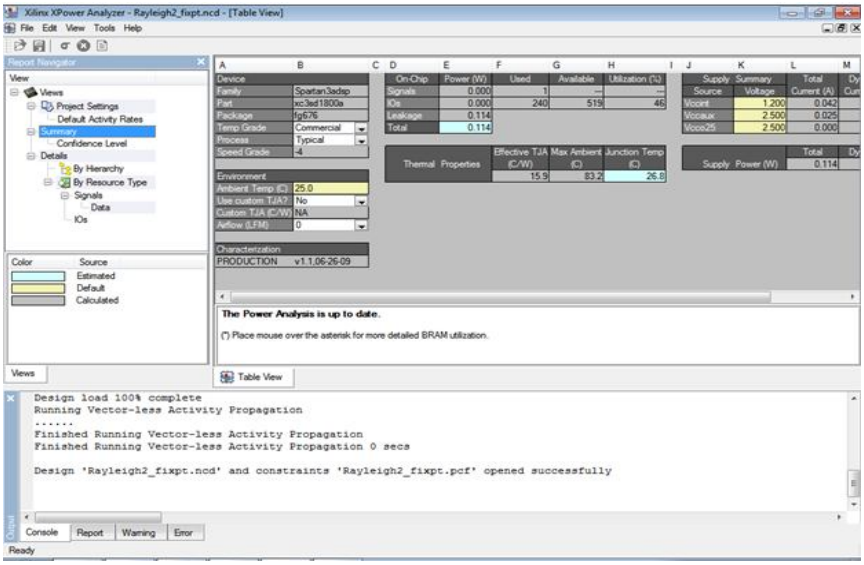

Fig.12 Power Analysis Report

Fig.9 and Fig.15 shows RTL Design of proposed model. This Register transfer level (RTL) model provides the synthesizable HDL model and presents the hardware look of the generated VHDL code. Fig.10 and Fig.16 shows technology view of proposed model. This Technology schematic diagram model gives the representation of components of a system through abstract and graphic symbols**.**

BER performance is optimized using MATLAB code and we are concentrating on power consumption performance using HDL coder. We want to analyze whether MATLAB optimized code will consumes less power or more. Mostly it is based on the number of bits and added noise. Therefore any data can be converted into bits. Simulation stage is needed to observe the simulation waveform in terms of binary value. In VHDL simulation result, we see the BER value and SNR values in binary and Hex as shown in Fig.11 and Fig.17. Current output BER in Hex is 27d9 as shown in Fig.11. According to MATLAB code simulation the corresponding BER is 0.0014 and conversion of 27d9H is also 0.0014.

B. Simulation of Video Signals

The simulation is carried out using five different video signals like cat video, scenevideoclip, vipcolorsegmentation video, vipfly video and viplane video signals are used to obtain the performance analysis of the DVB-T.

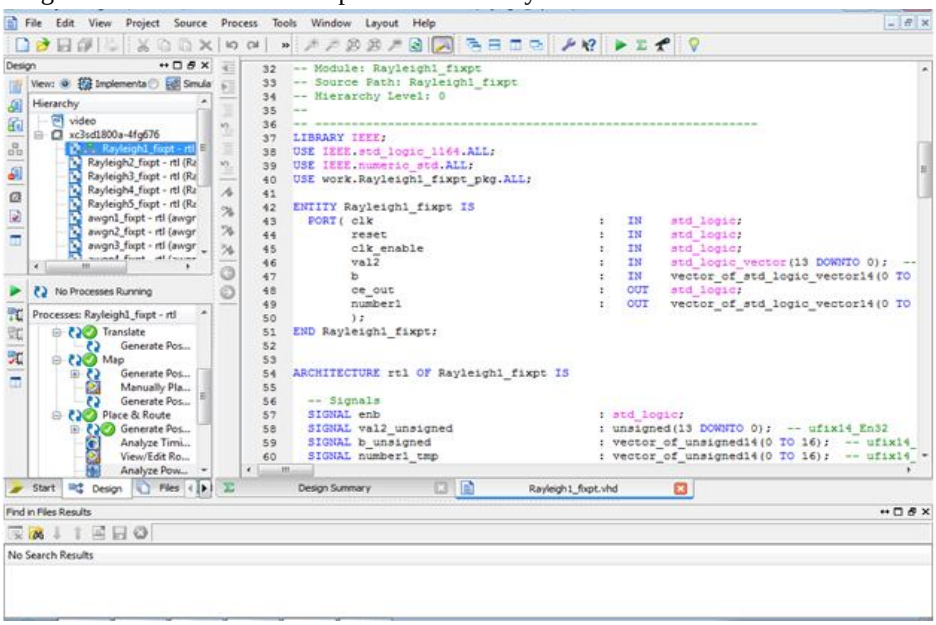

Fig.13 Generated VHDL Code for Video Inputs

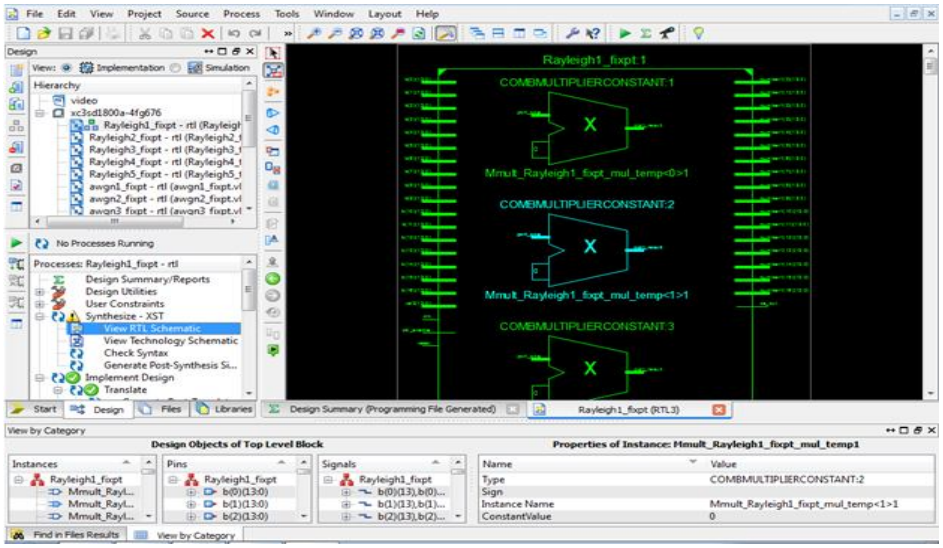

Fig.14 RTL Design

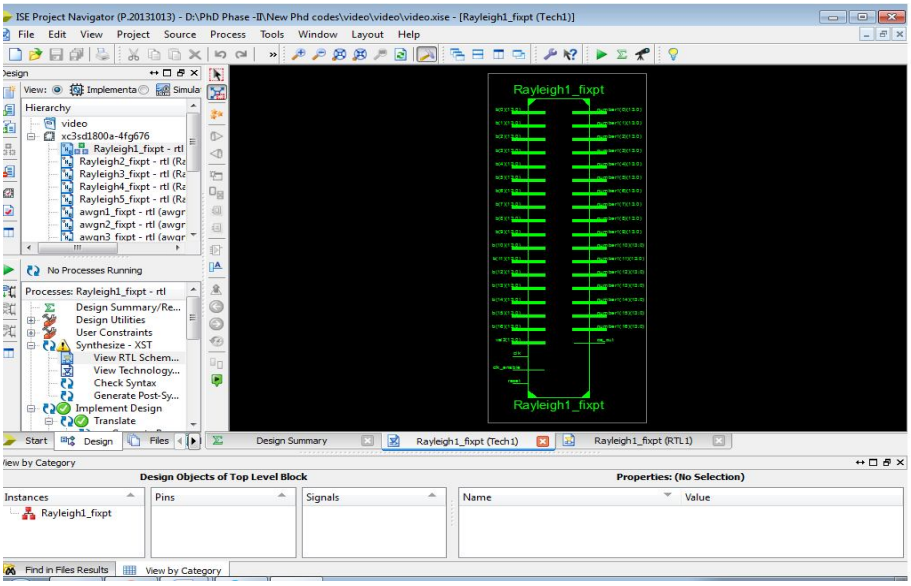

Fig.15 Technology View

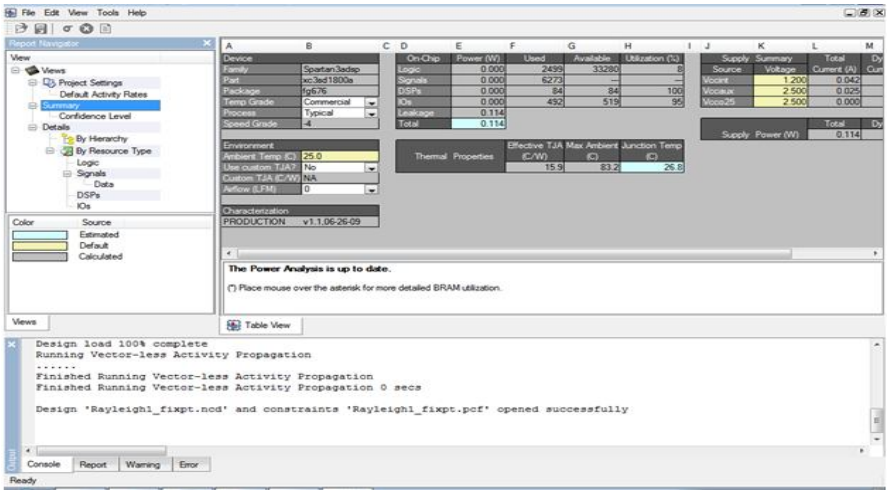

Fig.16 Power Analysis

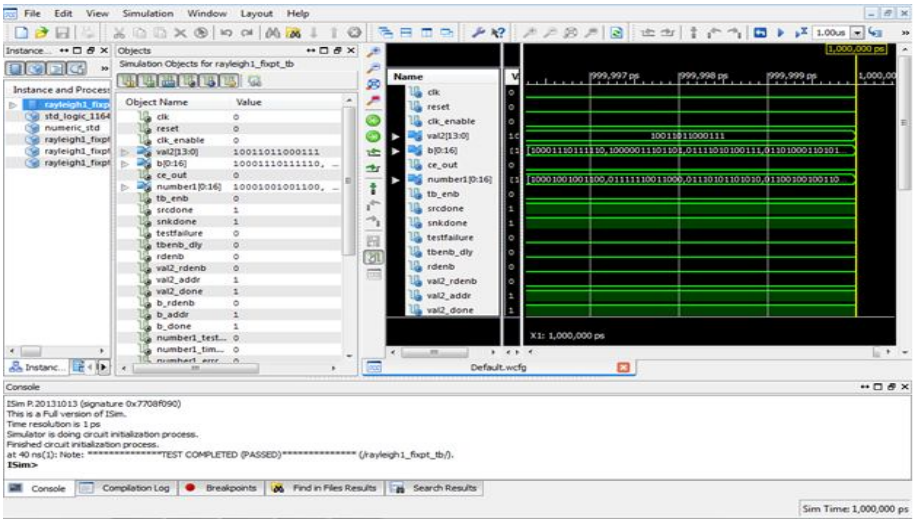

Fig.17 Simulation Results of SNR and BER Values in Binary

Fig.18, Fig 19 and Fig. 20 shows the device utilization summary and HDL resource utilization report.

Logic utilization	Used	Available	Utilization
Number of 4 input LUTs	2317	33290	6%
Number of occupied slices	1266	16640	7%
Number of slices containing only related logic	1266	1266	100%
Number of slices containing only unrelated logic	0	1266	0%
Total number of 4 input LUTs	2499	33280	7%
Number used as logic	2317	-	-
Number used as logic as route-thru	182	-	-
Number of bonded ICBs	492	519	94%
Number of DSP 48As	84	84	100%
Average fanout of non -clock nets	192	-	-

Fig.18 Device Utilization Summary

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1332	16640	8%
Number of 4 input LUTs	2464	33280	7%
Number of bonded IOBs	492	519	94%
Number of DSP48s	84	84	100%

Fig.19 Device Utilization Summary (estimated values)

```
Macro Statistics
# Multipliers                                      : 51
 14x14-bit multiplier                              : 17
 28x14-bit multiplier                              : 17
 42x14-bit multiplier                              : 17

=========================================================================
```

Fig 20 HDL Resource Utilization Report

V. CONCLUSION AND FUTURE WORK

In this research, first OFDM based DVB-T system is implemented using MATLAB and VHDL code is generated by means of HDL coder successfully. Synthesis and simulation is successfully carried out using Xilinx tool. It is observed that HDL coder offers the elapsed time to execute the code. The BER performance of the DVB-T system in 2k mode is analyzed for 4-QAM constellations using AWGN, Rayleigh and Rician channels with five different audio and video transmissions. In future work, Peak Average Power Ratio (PAPR) performance of DVB-T is proposed to be evaluated and suggest a PAPR reduction techniques like PTS (partial transmit sequence) and SLM (selected mapping) to improve performance.

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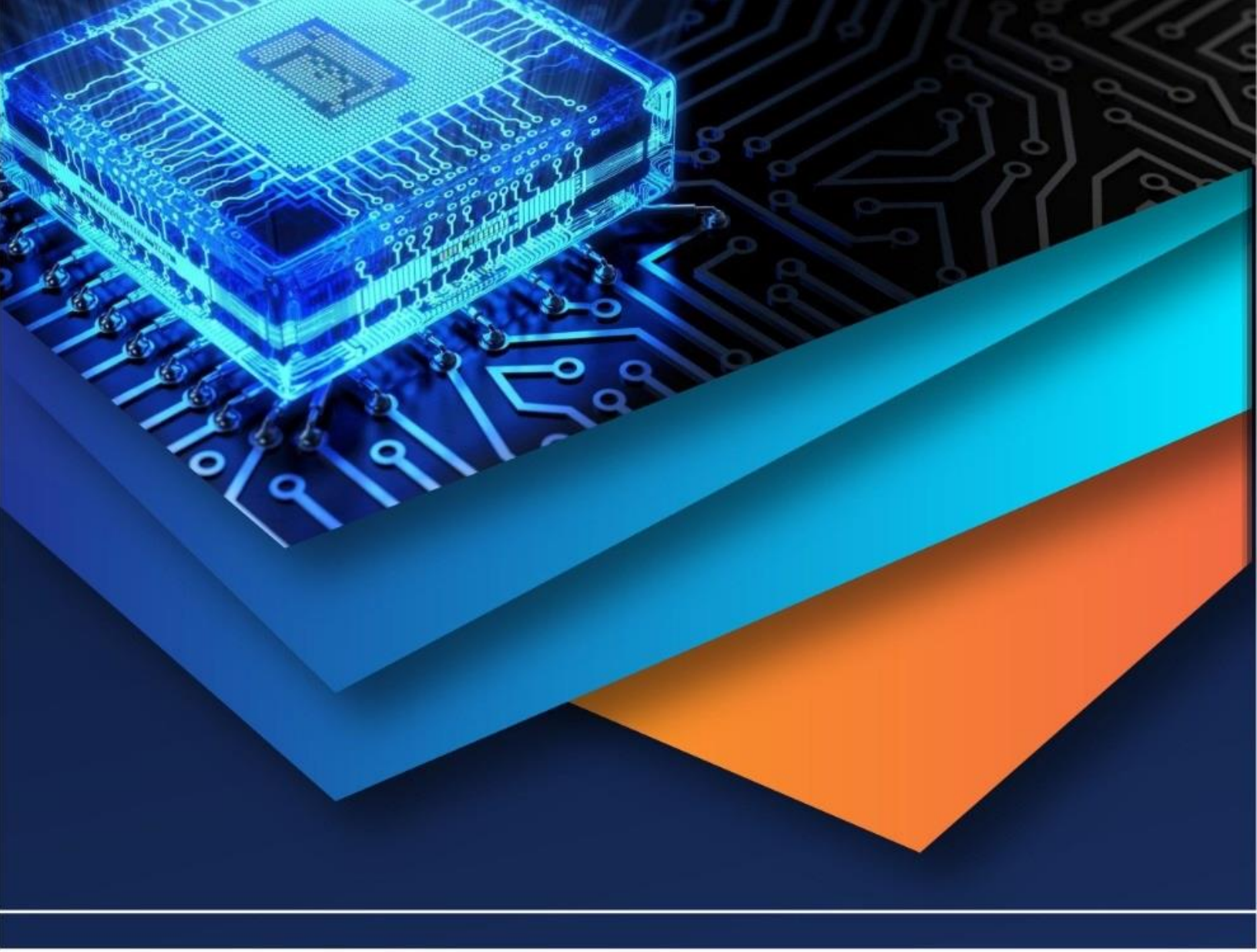

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