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## Certificate

*It is here by certified that the paper ID : IJRASET13369, entitled  
Design and Operational Synthesis of 64-bit Adder and Subtractor Unit using Delay  
Efficient Parallel Prefix Technique*

*by  
Akash Tiwari*

*after review is found suitable and has been published in  
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*Good luck for your future endeavors*

*By [Signature]*

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