



ISSN No. : 2321-9653

IJRASET

**International Journal for Research in Applied
Science & Engineering Technology**

IJRASET is indexed with Crossref for DOI-DOI : 10.22214

Website : www.ijraset.com, E-mail : ijraset@gmail.com

Certificate

It is here by certified that the paper ID : IJRASET4878, entitled
Design and Implementation of Logic Gates and Adder Circuits on FPGA Using ANN
by
Neelu Farha

after review is found suitable and has been published in
Volume 4, Issue V, May 2016
in

*International Journal for Research in Applied Science &
Engineering Technology*
(International Peer Reviewed and Refereed Journal)
Good luck for your future endeavors

By [Signature]

Editor in Chief, IJRASET



ISRA Journal Impact
Factor: 7.429



45.98
INDEX COPERNICUS



THOMSON REUTERS
Researcher ID: N-9681-2016



TOGETHER WE REACH THE GOAL
SJIF 7.429



ISSN No. : 2321-9653

IJRASET

**International Journal for Research in Applied
Science & Engineering Technology**

IJRASET is indexed with Crossref for DOI-DOI : 10.22214

Website : www.ijraset.com, E-mail : ijraset@gmail.com

Certificate

It is here by certified that the paper ID : IJRASET4878, entitled
Design and Implementation of Logic Gates and Adder Circuits on FPGA Using ANN
by
Ann Louisa Paul J

after review is found suitable and has been published in
Volume 4, Issue V, May 2016
in

*International Journal for Research in Applied Science &
Engineering Technology*
(International Peer Reviewed and Refereed Journal)

Good luck for your future endeavors

By [Signature]

Editor in Chief, IJRASET



ISRA Journal Impact
Factor: 7.429



45.98
INDEX COPERNICUS



THOMSON REUTERS
Researcher ID: N-9681-2016



TOGETHER WE REACH THE GOAL
SJIF 7.429



ISSN No. : 2321-9653

IJRASET

**International Journal for Research in Applied
Science & Engineering Technology**

IJRASET is indexed with Crossref for DOI-DOI : 10.22214

Website : www.ijraset.com, E-mail : ijraset@gmail.com

Certificate

It is here by certified that the paper ID : IJRASET4878, entitled
Design and Implementation of Logic Gates and Adder Circuits on FPGA Using ANN
by
Naadiya Kousar L S

after review is found suitable and has been published in
Volume 4, Issue V, May 2016
in

*International Journal for Research in Applied Science &
Engineering Technology*
(International Peer Reviewed and Refereed Journal)

Good luck for your future endeavors

By [Signature]

Editor in Chief, IJRASET



ISRA Journal Impact
Factor: 7.429



45.98
INDEX COPERNICUS



THOMSON REUTERS
Researcher ID: N-9681-2016



10.22214/IJRASET



TOGETHER WE REACH THE GOAL
SJIF 7.429



ISSN No. : 2321-9653

IJRASET

**International Journal for Research in Applied
Science & Engineering Technology**

IJRASET is indexed with Crossref for DOI-DOI : 10.22214

Website : www.ijraset.com, E-mail : ijraset@gmail.com

Certificate

It is here by certified that the paper ID : IJRASET4878, entitled
Design and Implementation of Logic Gates and Adder Circuits on FPGA Using ANN
by
Devika S

after review is found suitable and has been published in
Volume 4, Issue V, May 2016
in

*International Journal for Research in Applied Science &
Engineering Technology*
(International Peer Reviewed and Refereed Journal)
Good luck for your future endeavors

By

Editor in Chief, IJRASET



ISRA Journal Impact
Factor: 7.429



45.98
INDEX COPERNICUS



THOMSON REUTERS
Researcher ID: N-9681-2016



TOGETHER WE REACH THE GOAL
SJIF 7.429