

# RASET

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It is here by certified that the paper ID: IJRASET63345, entitled

Simultaneous Area and Latency Optimisation for Stochastic Circuit by D Flip-Flop
Insertion

by K. Deepa Rao

after review is found suitable and has been published in Volume 12, Issue VI, June 2024

in

International Journal for Research in Applied Science & Engineering Technology
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